1280 InGaAs Panel Detector user manual

1280×1024, 15μm,

A97AA15M1-B Type



Introduction

The 1280 × 1024 InGaAs area array detector is mainly composed of a low noise readout circuit (ROIC), a P-I-N structure InGaAs photosensitive chip and a primary thermoelectric cooler (TEC), and is packaged in metal form. This manual only describes the product A97AA15M1-B.

Main Parameter

Photoelectric Parameter

Parameter	Typ
Response spectral range(μm)*1	0.95 ±0.05~1.7 ±0.05
Pixel filling rate(%)	100
Peak quantum efficiency(%)	≥70@1.55μm
Peak detection rate*2(cm · Hz/w)	≥5× 1012
Peak sensitivity(A/W)	≥0.8
Effective pixel rate(%)*3	>99.5
Response heterogeneity(%)	≤5

Read-out way	IWR 、ITR 、CDS 、NDRO 、IMRO
Readout rate(MHz)	Range2~22
Read channel number	2 、4 、8，optional
Full frame frame rate(Hz) *4	100
Gain gear	3
Conversion gain(μV/e-)	1 (LG) 、16(MG) 、50 (HG)
Dynamic Range(dB) *5	≥55 (MG)

* 1 Focal plane temperature =25℃

*2 Focal plane temperature =20℃, high gain, integration time 10ms

* Under conditions near the optical signal half-well, the percentage of pixels whose response signal is less than 50% off the average value *4 Number of readout channels =8, readout mode IWR, readout rate 22MHz

*5 Focal plane temperature =20℃, open CDS

Mechanical Parameter

Parameter	Typ
Long × Wide × Height (mm)	38 ×38 × 8.1
Weight (g)	~45
Focal plane scale	1280 × 1024
Pixel center to center distance（ μ M)(μ m)	15
Pixel size(μ m)	15 × 15
Photosensitivearea(mm)	19.2 × 15.36

Usage environment and power consumption parameters

Parameter	Typ
Working temperature (℃)	-20~+60
Storage temperature(℃)	-40~+70
Typical power(W)*	<0.4

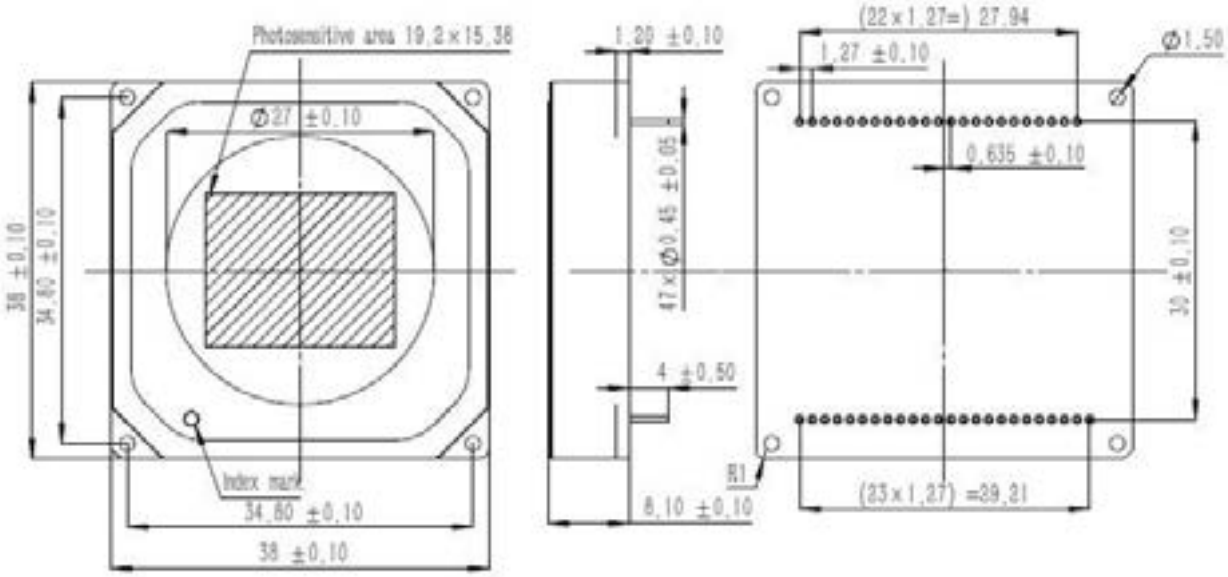
*TEC not enabled, ambient temperature=25 ℃, serial port configuration default state

Mechanical Parameter

The detector adopts the metal package form filled with atmospheric pressure high-purity nitrogen, metal shell FeNiCoSi alloy, surface plating Ni / Au layer, the window welding method for the In-system brazing, the cover form for resistance welding. The external dimensions of the detector are 38mm (L)×38mm (W)×8.1mm (H). There are 47 Φ0.45mm pins from the bottom of the housing, which are arranged in a double-sided single-row zigzag pattern, and the spacing between the pins in a single row is 1.27mm, which are used for the input of focal plane power supply and commands, the focal plane detection signals, the electrical lead-out of temperature

sensors, and the connection of the thermoelectric cooler. The detector has one Φ1.5mm through-hole at each corner for fixation.

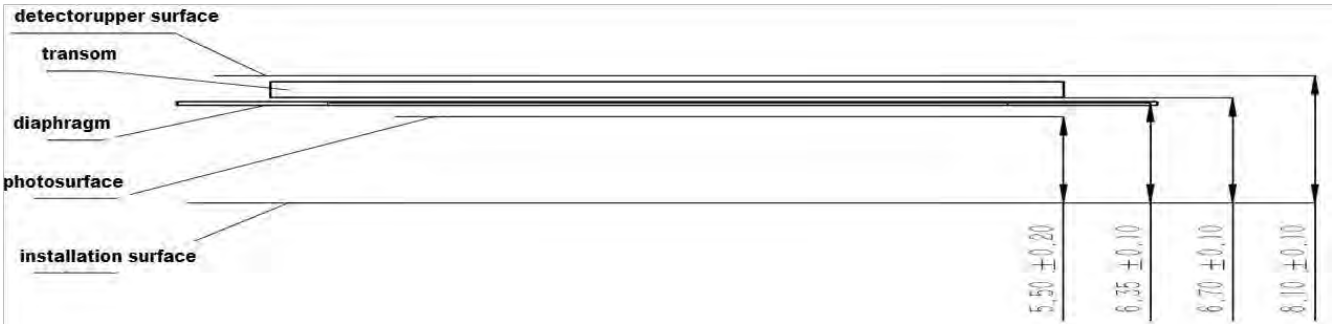
The mechanical interface appearance and dimensions are shown below:



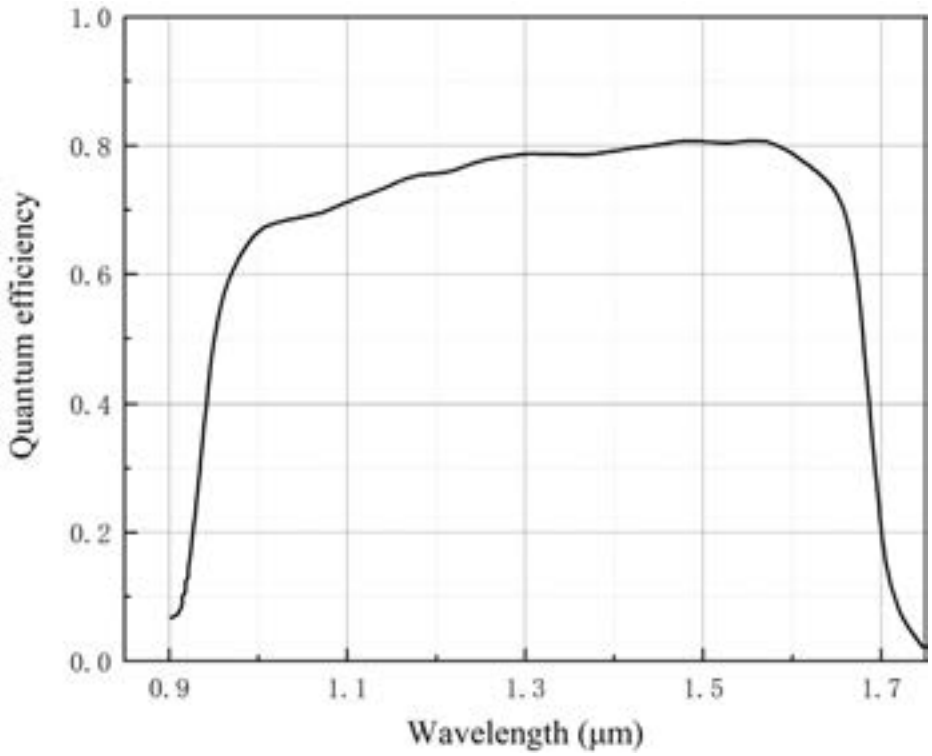
Optical Parameters

Optical structure

The detector adopts a 1280×1024 InGaAs focal plane with 15μm pixel center distance, square shape, and 15μm×15μm sensing size. The designed distance between the detector photosensitive surface and the upper surface of the detector structure is 2.6±0.2mm, the designed distance between the detector photosensitive surface and the lower surface of the optical window is 1.2±0.2mm, and the designed distance between the detector photosensitive surface and the lower surface of the diaphragm is 0.85±0.2mm. The optical window material is sapphire with thickness of 0.6±0.02mm, refractive index of 1.76, AR film coated on the surface, transmittance >95% in the responsive band, transmittance area of the optical window is φ27mm, and the diaphragm transmittance size is 19.8mm×16mm. The center of the photosensitive surface is located in the center of the detector, the relative positional shift is ≤0.05mm, and the relative rotational displacement is ≤0.02mm.

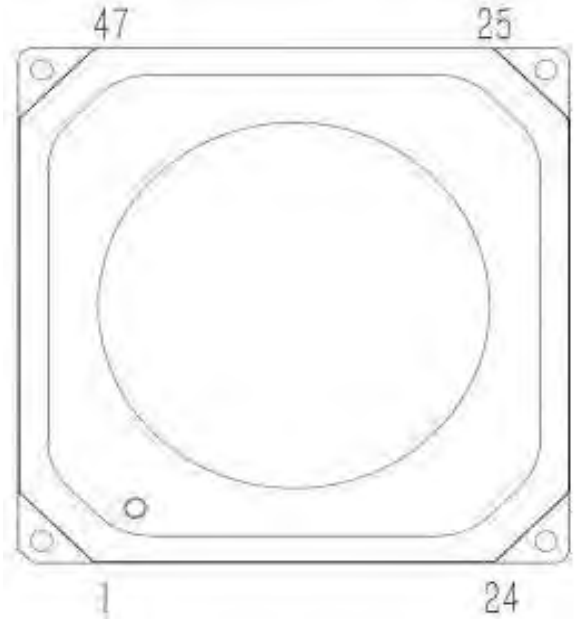


Quantum efficiency (typical value)



Electrical Characteristics

Detector Pin Diagram



Detector pin description

PIN	Item	Input/ Output	Function	Reference Value
1	NC		Empty leg, not connected	
2	CLK	Input	Detector master clock	Digital voltage High level 3.3V，Low level 0V
3	SERDAT	Input	Register command word	Digital voltage High level 3.3V, low level 0V
4	NC		An empty foot must be in the air	
5	ROW ST	Output	Detector master clock	
6	ST	Output	Frame output identifier	
7/8	TS		The temperature sensor measures the electrical resistance value through two pins to feedback the operating temperature of the focal plane	
9/10	NC		Identical 1	
11	VOUT8	Output	The eighth channel in the eight-channel output mode	
12	VOUT7	Output	The seventh channel in the eight-channel output mode	
13	VOUT6	Output	The sixth channel in the eight-channel output mode	
14	VOUT5	Output	The fifth channel in the eight-channel output mode	
15	VOUT4	Output	The fourth channel in the eight-channel, four-channel output mode	
16	VOUT3	Output	The third channel in the eight-channel, four-channel output mode	
17	VOUT2	Output	The second channel in the eight-channel, four-channel, two-channel output mode	
18	VOUT1	Output	The first channel in the eight-channel, four-channel, two-channel output mode	
19	GNDA2		Analog power ground	
20	VDDA2	Input	Analog power	Analog 3.6V，Driving

				current >90mA
21	VDDL	Input	Analog power	Analog 3.6V，Driving current >90mA
22	GNDL		Analog power ground	
23	CASE			Recommended grounding
24	TEC-		Thermoelectric cooler connection pin -	
25	TEC+		Thermoelectric cooler connecting pin + , + pin connected to the high potential for cooling, connected to the low potential for heating	

PIN	Item	Input/ Output	Function	Reference Value
26	NC		Identical 1	
27	SUBPV	Input	Detector common terminal	Analog 3.2V，Driving current >20mA
28	VRIN	Input	Reference power input	
29	NC		Identical 4	
30	VBLM	Input	Anti-corona voltage external input	Internally generated, supports external tuning
31	VTEMP	Output	Integrated temperature sensing voltage output	Voltage gain-6mV/K
32/33	VDDA3	Input	Analog power	Analog 3.6V，Driving current >200mA
34/35	GNDA3		Analog power ground	
36	GNDA1		Analog power ground	
37	VDDA1	Input	Analog power	Analog 3.6V，Driving current >90mA
38/39	NC		Identical 1	
40	VD33	Input	Digital input/output power supply	Analog 3.3V，Driving current >30mA
41	VDD	Input	Digital power	Analog 1.8V，

				Driving current >30mA
42	VG33	Input	Analog power ground	
43-45	NC		Identical 1	
46	INT	Input	Integral control signal	Digital voltage High level 3.3V, low level 0V
47	RESET	Input	External reset signal	Digital voltage High level 3.3V, low level 0V

Attention：

The DC input directly affects the overall noise of the detector, so the ripple noise of the DC input power supply has the following requirements:

1) Voltage ripple noise requirements of each power supply:：

a) VDDA1~3: <1mV;

b) VDDL: <10mV;

c) VD33: <10mV;

d) VDD: <10mV;

2) Load requirements on the signal output terminals (VOUT1 to VOUT8)： Cload<25pF; Rload>100kΩ;

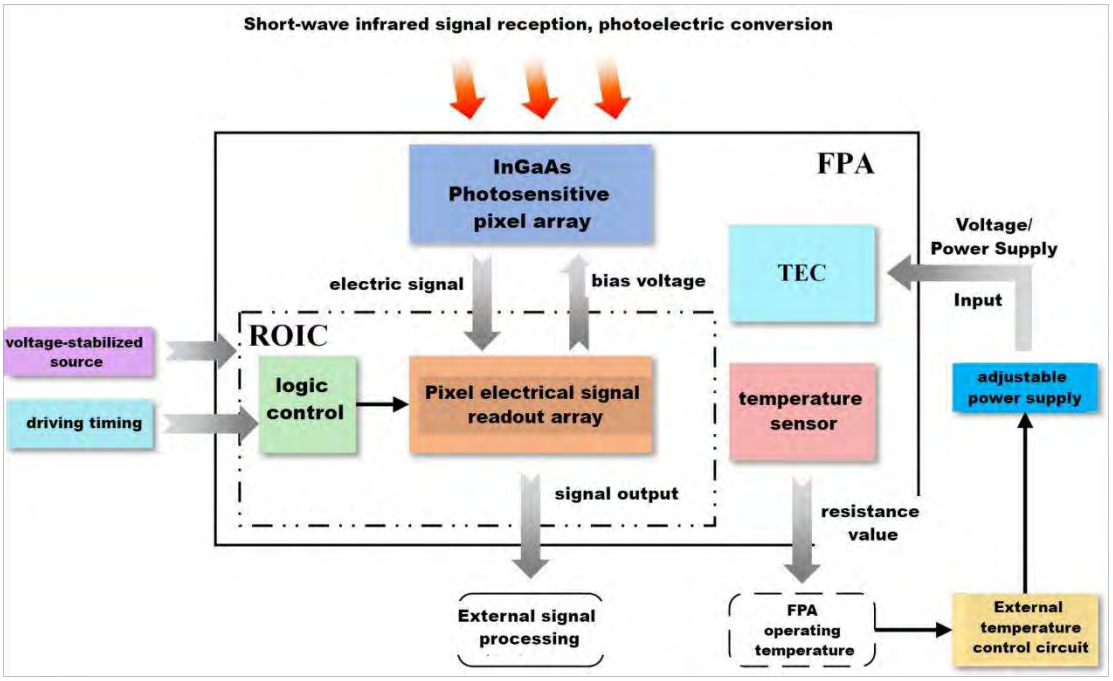
3) Logic output signal range: logic output signal is high and low level digital signal,，including

a) low level： 0~0.3V;

b) High level： (VD33-0.3V)~VD33;

c) Logical output load requirements： Cload<15pF。

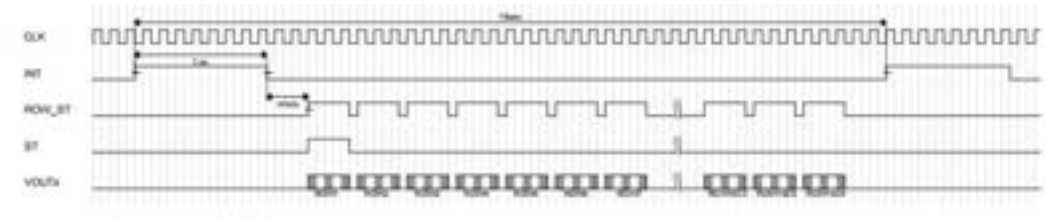
Schematic diagram of detector working principle and connection mode



Detector timing specification

ITR mode

The read-out circuit drive timing pulse diagram is as follows:



Timing detail：

a) The serial port command word input needs to be completed before the integration starts;

b) INT as an integral time control signal, high and low level length are integer Tclk；

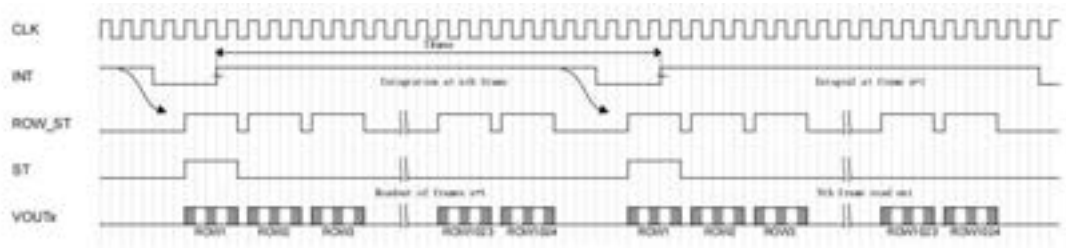
c) After the current frame integration Tint is completed, it is necessary to read the integral signal after Thold (149 Tclk). In the process of reading the current frame signal, the first line is read out line by line. After each line is read out, the next line of integral signal is read out after Td (37 Tclk) until the whole signal is read out.

d) When the current frame integration signal begins to be read out, the detector synchronously outputs ST and ROW_ST voltage signals, where ST is the frame output flag; ROW_ST is the line output flag, the high level width is Tclk×C/N, and the interval between adjacent high levels is Td until the integrated signal reading is completed.

e) In each output, the integrated signal of a pixel needs to pass through a master clock Tclk, and Tout=C×R/N×Tclk+(R-1)×Td, where C is the number of columns, R is the number of rows, and N is the number of output channels; Working frame period Tframe= Tint+Thold +Tout

IWR mode

The read-out circuit drive timing pulse diagram is as follows:



f) Detailed explanation of timing:

g) a) The serial port command word input needs to be completed before the integration starts;

h) b) In this mode, the integration of the current frame pixel signal and the readout of the previous frame integral signal are completed simultaneously in one frame cycle.

i) c) INT as an integral time control signal, the length of high and low level is an integer Tclk, and the low level width must be greater than 45 Tclk;

j) d) After the current frame integration Tint is completed, the integration signal readout needs to go through Thold (149 Tclk). During the signal readout process, the integration signal readout starts line by line from the first line. After the readout of each line, the integration signal readout of the next line starts through Td (37 Tclk) until the whole signal readout is completed.

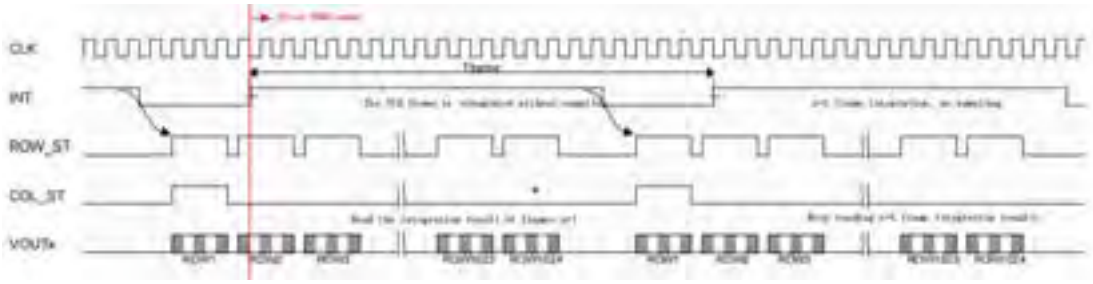
k) e) When the current frame integration signal begins to be read out, the detector synchronously outputs ST and ROW_ST voltage signals, where ST is the frame output mark; ROW_ST is the line output flag, the high level width is Tclk ×C/N, and the interval between adjacent high levels is Td until the integrated signal reading is completed.

l) f) In each output, the integrated signal of a pixel needs to pass through a master clock Tclk, and Tout=C ×R/N ×Tclk+(R-1)×Td, where C is the number of columns, R is the number of rows, and N is the number of output channels;

m) g) The frame period is approximately equal to the readout time, and the overall frame period requirements are: Tframe≥ Thold +Tout.

NDRO mode

The read-out circuit drive timing pulse diagram is as follows:



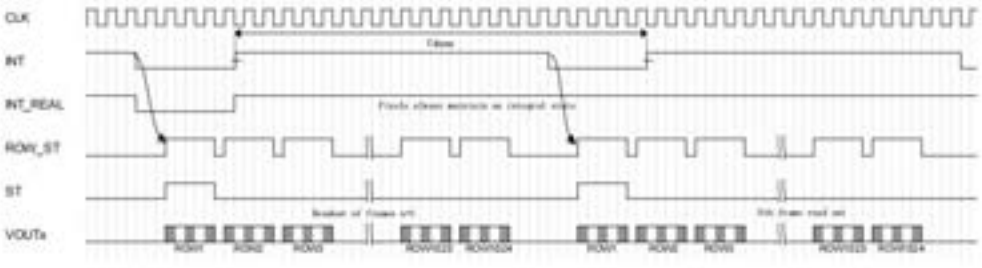
a) In the serial port command configuration, after the code bit of the control NDRO read out is set to the NDRO mode, the detector continues to integrate according to the IWR read out mode, but does not perform signal sampling.

b) The output signal value is always maintained as the integral signal of the last frame before entering the NDRO mode, and the frame holding signal is repeatedly output.

c) After the coding bit of the control NDRO readout is set to turn off the NDRO mode, the detector enters the IWR readout mode, but the frame still outputs the hold signal, and the next frame outputs the IWR normal integration signal.

IMRO mode

The read-out circuit drive timing pulse diagram is as follows:



Detailed explanation of timing：

a) In the configuration of serial command word, after the code bit of the control IMRO read out is set to IMRO mode, the detector continues to sample the signal according to IWR mode, but the integration is continuous, and the output signal value is the result of the integration in the previous Tframe.

b) After the IMRO mode is disabled, the probe enters the IWR read mode.

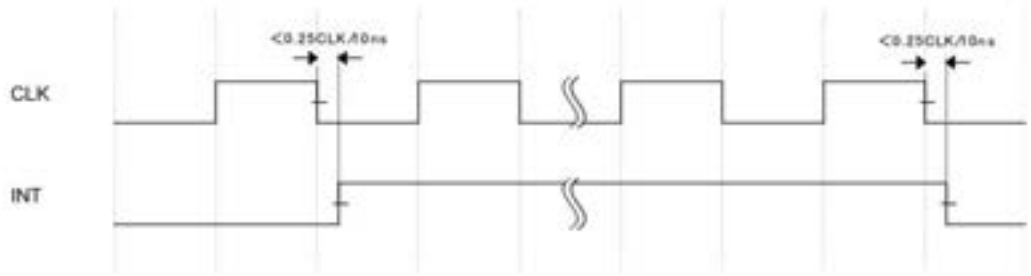
Attention：

a) At the beginning of each frame, the command word is not entered, and the parameter Settings will be consistent with the previous frame, and directly enter the integration process;

b) Under the typical clock frequency of 10MHz, the position of the rising edge of INT integral time is suggested to be 10ns after the falling edge of the master clock Tclk.

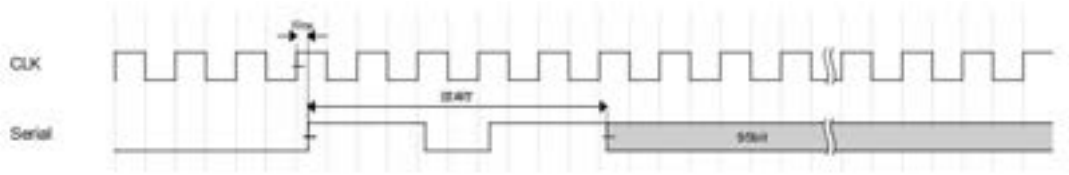
c) For both NDRO and IMRO modes, if the register is configured to enter both IMRO and NDRO modes at the same time, the detector will only read in IMRO mode, that is, IMRO mode has a higher priority than NDRO mode.

d) The selection of ITR and IWR mode is automatically determined by the circuit according to the length of the set integration time. When the sum of INT high level + low level time is not enough to meet the reading of a frame full amplitude signal Tint+Thold <Tout, the IWR mode is automatically converted to ITR mode.



Serial port command word configuration

Serial port command word configuration sequence diagram



Attention：

a) It is recommended that the first rising edge of the SERIAL command word mark 5b '11011 be set at 10ns behind the rising edge of the master clock Tclk.

b)After the serial port command word is configured, it is updated on the next INT ascending edge.

Command word each definition

Order	Item	Function	Length	Recommended value（1 is high and 0 is low）
1	Start[4:0]	Command Word Start Flag Bit	5bit	5’b11011
2	Gain[1:0]	Gain size control	2bit	2’b00
3	UPcol	Image flip control	1bit	1’b1
4	UProw		1bit	1’b1
5	TEST_ 1	Test control	1bit	1’b1
6	SizeA	Preset Size	1bit	1’b1
7	SizeB	Window Control	1bit	1’b1
8	Cstart[9:0]		10bit	10’b0
9	Cfinal[9:0]	Custom window opening control：	10bit	10’b0
10	Rstart[9:0]	Window start and stop row and column coordinates	10bit	10’b0
11	Rfinal[9:0]		10bit	10’b0
12	PWctrl[1:0]	Power consumption control	2bit	2’b01
13	NBOUT[1:0]	Number of output channels control	2bit	2’b11
14	TEST_2[1:0]	Test control	2bit	2’b00
15	ICTL_ APW[2:0]	Pixel power control	3bit	3’b010
16	ICTL_ BUF [1:0]	Driver power control	2bit	2’b01
17	ICTL_AK[1:0]	Common Circuit Power Control	2bit	2’b01
18	ICTL_OUT[1:0]	Output Op-Amp Power Control	2bit	2’b10
19	TEST_3[2:0]	Test Control	3bit	3’b101
20	BLM_EN	Anti-Halo Enable Control Bit	1bit	1’b1
21	BLM_CTL[2:0]	Anti-Halation Voltage Adjustment Control	3bit	3’b010
22	TEST_4[4:0]	Test Control	5bit	5’b01001
23	TCDS[3:0]	TCDS clock count control	4bit	4’b0110
24	TEST_5[10:0]	Test Control	11bit	11’b0
25	CDS	CDS mode control bits	1bit	1’b1
26	NDRO	NDROmode control bits	1bit	1’b0
27	IMRO	IMROmode control bits	1bit	1’b0
28	TEST_6[2:0]	Test Control	3bit	3’b010

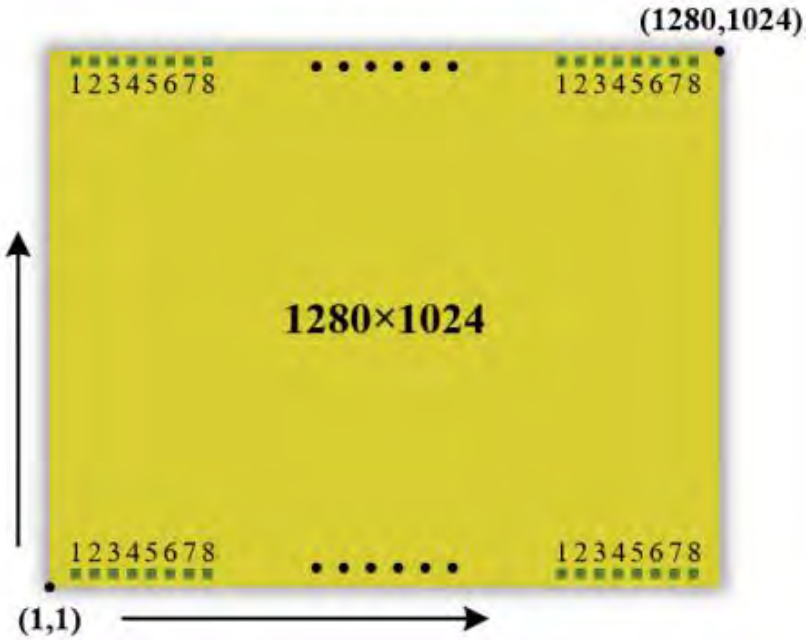
Gain size controlGain[1:0]

Gain[1]	Gain[0]	Corresponding Gain
0	0	HG（default）
0	1	MG
1	0	LG
1	1	Approximate LG

Image flip controlUPcol 、UProw

When the bottom left is pin # 1, the bottom left is read from the origin (1, 1) to the upper right (1280, 1024) by default.

UP_{col}	UP_{row}	Image output sequence		
0	0	Top right starting point, right to left, top to bottom (default)		
0	1	Bottom right，	Right to left，	bottom to top
1	0	Top left,	left to right,	top to bottom
1	1	Bottom left，	left to right，	bottom to top



*Note： The figure above is a schematic diagram of the readout sequence in the 8-channel readout when pin 1 is in the lower left.

Preset size window opening controlSizeA 、SizeB

SizeA	SizeB	Window size
1	1	Full frame 1280×1024 (default)
1	0	Central area 1280×720
0	1	The central area is 1024 x 1024
0	0	Custom size

Customize window opening Settings

a) The number of Windows is independent of the number of output channels. The starting line is 0≤Rstart ≤1020, and the ending line is 0≤Rfinal≤1023.
b) Two-channel output: NBOUT[1:0]=2 'b00 or 2' b01
Start column: 2 x Cstart, 0≤Cstart≤636;
Column of the end point: 2 ×Cfinal+1, 3≤Cfinal≤639;
Minimum window size: 4 (row R) x 8 (column C)
c) Four-channel output:NBOUT[1:0]=2’ b10
Start column： 4 ×Cstart ， 0≤Cstart≤316；
Column of the end point： 4 ×Cfinal+3 ， Cstart +3≤Cfinal≤319；
Minimum window size： 4 (row R) ×16 (column C)
d) Eight-channel output：NBOUT[1:0]=2’ b11
Start column： 8 ×Cstart ， 0≤Cstart≤156；
Column of the end point： 8 ×Cfinal+7 ， Cstart +3≤Cfinal≤159；
Minimum window size： 4 (row R) x 32 (Column C)

Power consumption controlPWctrl[1:0]

Pctrl[1]	Pctrl[0]	Power consumption ratio
1	1	200%
1	0	150%
0	1	100%（default）
0	0	50%

Number of output channels selectedNBOUT[1:0]

NBOUT [1]	NBOUT [0]	Output channel number
1	1	Eight-channel (default)
1	0	four-channel
0	1	two-channel
0	0	two-channel

Pixel power control ICTL_ APW[2:0]

ICTL_APW[2]	ICTL_APW[1]	ICTL_APW[0]	Power consumption ratio
0	0	0	33%
0	0	1	67%
0	1	0	100%（default）
0	1	1	133%
1	0	0	167%
1	0	1	200%
1	1	0	234%
1	1	1	267%

BUF power consumption control ICTL_BUF[1:0]

ICTL_BUF[1]	ICTL_BUF[0]	Power consumption ratio
1	1	200%
1	0	150%
0	1	100%（default）
0	1	66%

Common circuit power consumption controlICTL_AK[1:0]

ICTL_AK[1]	ICTL_AK[0]	Control signal rise/Falling edge time
1	1	350ns
1	0	0.5μs
0	1	0.8μs（default）
0	0	1.5μs

Output power control ICTL_OUT[1:0]

ICTL_OUT[1]	ICTL_OUT[0]	Power consumption ratio
1	1	120%
1	0	100%（default）
0	1	80%
0	0	60%

Integral preparation time controlT_READY[2:0]

T_READY[2]	T_READY[1]	T_READY[0]	Integration preparation time
0	0	0	93 μ s
0	0	1	50 μ s
0	1	0	20 μ s
0	1	1	4.3 μ s
1	0	0	2.2 μ s
1	0	1	1.1 μ s（default）
1	1	0	0.5 μ s
1	1	1	170ns

Anti-halo function controlBLM_EN and BLM_CTL[2:0]

BLM_EN	BLM_CTL[2:0]	VBLMvoltage values
0	XXX	0V
1	000	0.8V
1	001	0.93V
1	010	1V（default）
1	011	1.07V
1	100	1.15V
1	101	1.21V
1	110	1.28V
1	111	1.35V

TCDS clock number control signalTCDS[3:0]

TCDS	TCDSNumber of clocks	TCDS	TCDSNumber of clocks
0000	0Tclk	1000	352Tclk
0001	44Tclk	1001	396Tclk
0010	88Tclk	1010	440Tclk
0011	132Tclk	1011	484Tclk
0100	176Tclk	1100	528Tclk
0101	220Tclk	1101	572Tclk
0110	264Tclk（default）	1110	616Tclk
0111	308Tclk	1111	660Tclk

CDSMode switch

CDS	Output mode
0	Non-cds mode output
1	CDS Mode output (default)

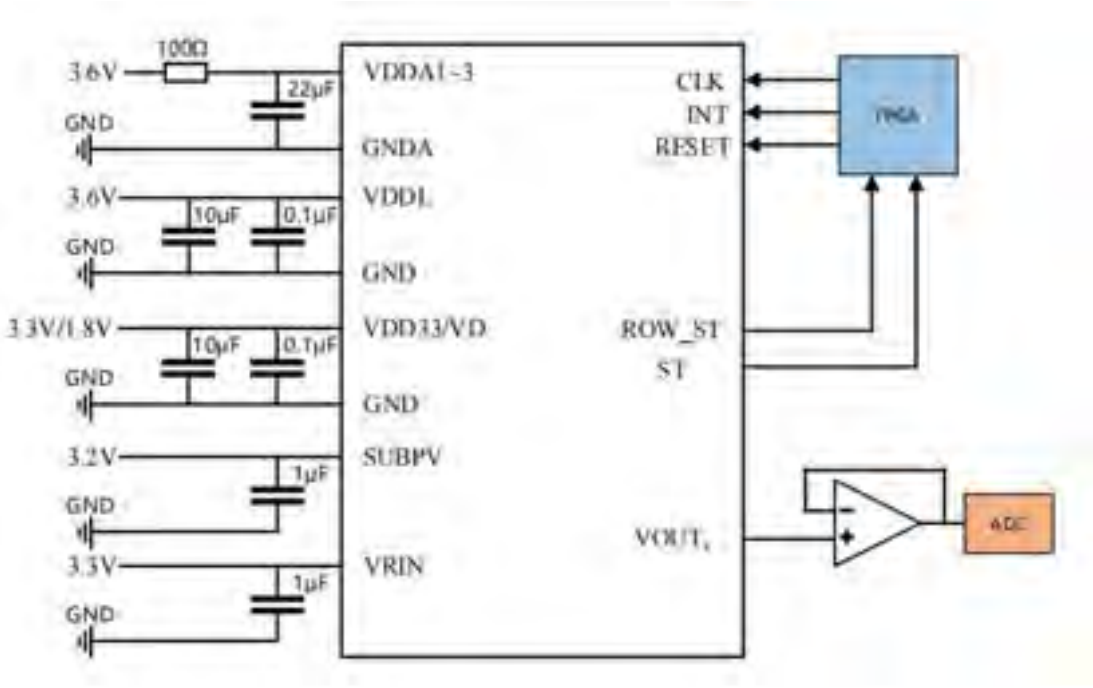
NDROMode switch

NDRO	Output mode
0	Non-ndro mode output (default)
1	NDRO mode output

IMROMode switch

IMRO	Output mode
0	Non-imro mode output (default)
1	IMRO mode output

Detector peripheral recommended circuit diagram



Thermal parameters

Thermoelectric Cooler Characteristics

The detector is integrated with a primary thermoelectric cooler (TEC), the center of the cooling surface is the center of the lower surface of the detector, and the cooling area should be ≥23mm×23mm, its performance parameters are shown in the following table:：

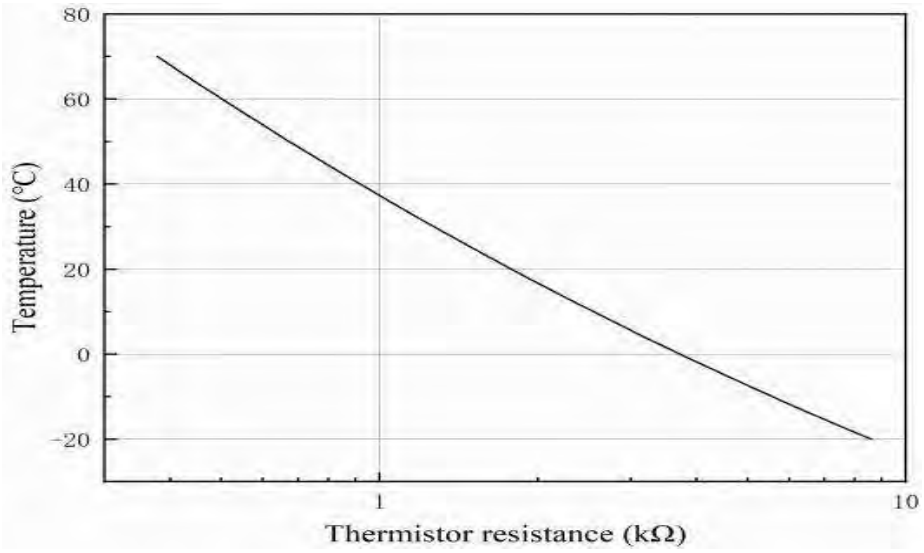
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Performance	Value
Maximum temperature difference between hot and cold surfaces(△Tmax/℃) *	20
Maximum load current allowed（ITEC-max/A）	1
The maximum load voltage allowed（VTEC-max/V）	2.7
AC impedance (including AC resistance) （ACR/Ω)	1.67- 1.98

performance index refers specifically to the temperature difference between the focal plane and the heat dissipation surface of the package structure

Temperature Sensor Characteristics

The detector uses a thermistor as a temperature sensor, and the corresponding relationship between the resistance value and temperature in the working temperature is shown in the following figure:：



The corresponding relationship between thermistor values and typical values of temperature is shown in the following table:

Temperature(℃)	Resistance（kΩ)	Temperature(℃)	Resistance（kΩ)
-20	8.608	30	1.268
-15	6.909	35	1.077
-10	5.587	40	0.918
-5	4.549	45	0.786
0	3.729	50	0.674
5	3.075	55	0.581
10	2.55	60	0.502
15	2.126	65	0.435
20	1.782	70	0.378
25	1.5		

The corresponding relationship between thermistor resistance and temperature is as follows:

$$\frac{1}{(T_1+273.15)}=\frac{\ln\left(\frac{R_1}{R_2}\right)}{B}+\frac{1}{(T_2+273.15)}$$

T1: test target temperature (unit: ° C)
T2: reference point temperature, unit: ℃, the typical value of the reference temperature within -20~70℃ is 10 or
At 40 ° C, a reference temperature value close to the target temperature should be selected
R1: T1 thermistor resistance, unit: kΩ
R2: Thermistor resistance corresponding to T2, unit: kΩ
B: Thermal sensitivity coefficient, the typical value of B10/40 in -20~70℃ is 3019.6 (deviation ±2%), by
The temperature deviation calculated for this typical value is ±0.5 ° C
Attention：
a) During TEC installation, pay attention to the new resistance introduced by the external electrical structure. If the new resistance exceeds 10% of the TEC resistance, the I-V curve needs to be proofread again;
b) If you need higher measurement accuracy in a small temperature range, you can calculate the B value according to the requirements;
c) Before starting the TEC, ensure that the temperature sensor is working properly, that the heat dissipation surface is in full contact with the heat sink, that the heat dissipation surface is not smaller than the required area, and that the heat sink is working properly. Do not install heat dissipation before starting the TEC
Turn on TEC when the device or radiator is not working;
d) When the TEC is turned on for the first time, the current or voltage should be gradually loaded starting from 0A or 0V, while the temperature is monitored
The degree changes until the preset temperature is reached;
e) Since the performance of the detector is affected by temperature, TEC should be turned on first until the temperature is stable before the detector is turned on.
It is not recommended that the detector work in the environment of temperature change;
f) When the detector is not working, the power supply to TEC should be stopped to extend the service life of TEC;
g) The cooling and heating effect of the detector is related to the ambient temperature, power supply performance and heat dissipation state
According to their own use of the environment and the performance requirements of the detector to carry out a reasonable collocation of heat dissipation system.

Support

Question	Possible causes	Solution
The detector VOUT signal output is abnormal	The power is not supplied or is abnormal	Check whether each power supply conforms to the electrical requirements in the operation manual
	Timing exception	etector timing pulse width should be modulated as recommended in the operator's manual
	Integration time is short or light is strong	Change the gain gear when increasing the integral according to the timing constraints
	Intensity saturation	Shorten the integration time, change the gain gear, and increase the filter
Detector output signal noise is too large	Power supply ripple noise	The ripple noise of the DC power supply shall be supplied according to the electrical requirements in the user manual
	Thermoelectric refrigerator pin reverse connection	The temperature sensor is used to detect whether there is a reverse connection
	Back-end electronic circuit noise introduction	Check board level circuit structure layout and circuit noise