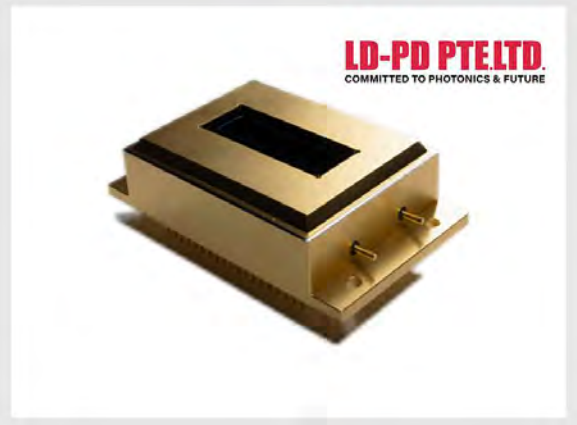
512×1 InGaAs Area Array Detector



Description

The Model L055125M2-A InGaAs Linear Detector is mainly composed of a 512×1 InGaAs photosensitive chip, a Read-Out Integrated Circuit (ROIC), and a two-stage Thermoelectric Cooler (TEC). It adopts a metal packaging design and features extended wavelength range and selectable multi-level gain. This detector is applicable to fields such as short-wave infrared imaging, industrial inspection, and color sorting.

Features

- Ultra-broad spectral range
- High spectral flatness
- High optical power

Key Parameter

Main optoelectronic specifications

Parameter	Typical Value
Response Spectral Range (μm)*¹	1.30 ±0.05 ~ 2.50 ±0.05
Peak Quantum Efficiency (%)	≥60
Dark Current Density (μA/cm²)*¹	<5
Effective Pixel Rate (%)*²³	≥98
Response Non-Uniformity (%)*³	<8
Readout Mode	IWR, ITR, optional
Readout Speed (MHz)	Single channel 10
Max Frame Rate (fps)	20k
Gain Levels	8
Saturation Voltage (V)	1.6
Conversion Gain (nV/e⁻)	Gain Level1: 16000

	Gain Level 2: 8000 Gain Level 3: 4000 Gain Level 4: 2665 Gain Level 5: 1775 Gain Level 6: 840 Gain Level 7: 325 Gain Level 8: 160

*1 Focal Plane Temperature = -20℃

*2 Percentage of pixels where the pixel response signal deviation from the average value is within a certain range

*3 Test Conditions: Focal Plane Temperature = -20℃, Gain at Level 8, Integration Time = 0.5ms

Mechanical Parameter

Parameter	Typical Value
Length × Width × Height (mm³)	55 ×32.6 × 13
Weight (g)	~78
Focal Plane Array Size	512 × 1
Pixel Pitch (μm)	25
Pixel Size (μm²)	25 ×250
Active Area (mm²)	12.8 ×0.25

Operating Environment & Power Consumption Spec

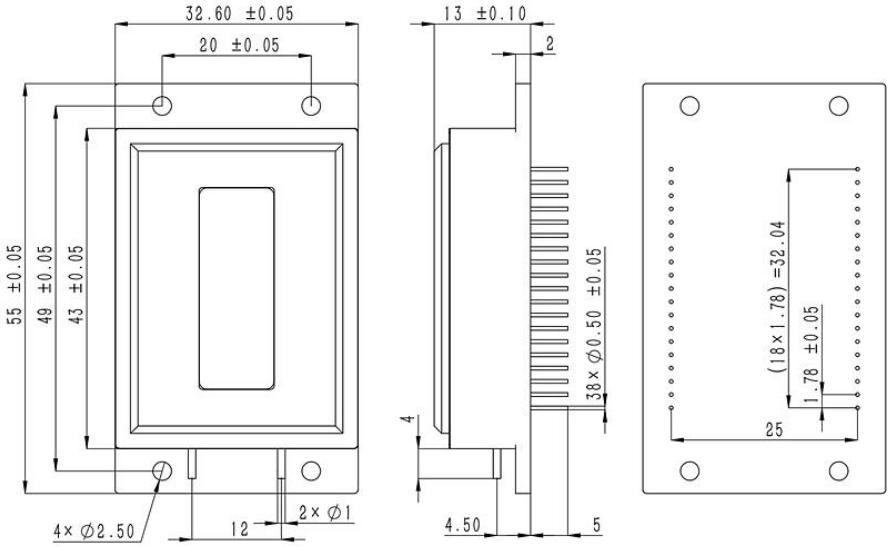
Parameter	Typical Value
Operating Temperature (°C)	0~+35
Storage Temperature (°C)	-5~+40
Typical Power Consumption (W)	<0.15

TEC Disabled, Ambient Temperature = 25℃, Number of Readout Channels = 8, Power Consumption Control Gear = 100%

Mechanical Specification

This detector adopts a metal packaging design, filled with high-purity nitrogen at atmospheric pressure. The metal shell is made of FeNiCoSi alloy, with a Ni/Au electroplated layer on the surface. The window is bonded via adhesive, and the cover is sealed by resistance welding. The external dimensions of the detector are 55mm (Length) × 32.6mm (Width) × 13mm (Height).

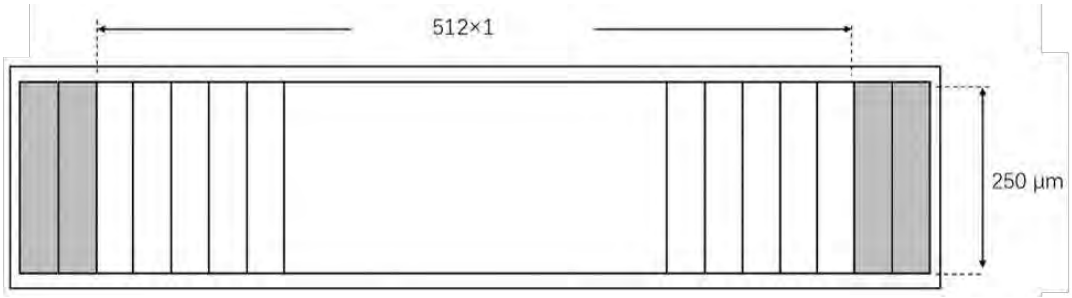
Thirty-eight pins with a diameter of Φ0.5mm are led out from the back of the shell, with a pin pitch of 1.78mm. These pins are used for the input of focal plane power supply and commands, as well as the electrical lead-out of focal plane detection signals and temperature sensor signals. Two pins with a diameter of Φ1.0mm on the side are used for connecting the thermoelectric cooler (TEC). Four through-holes with a diameter of Φ2.5mm are distributed on both sides of the package for fixing the detector.



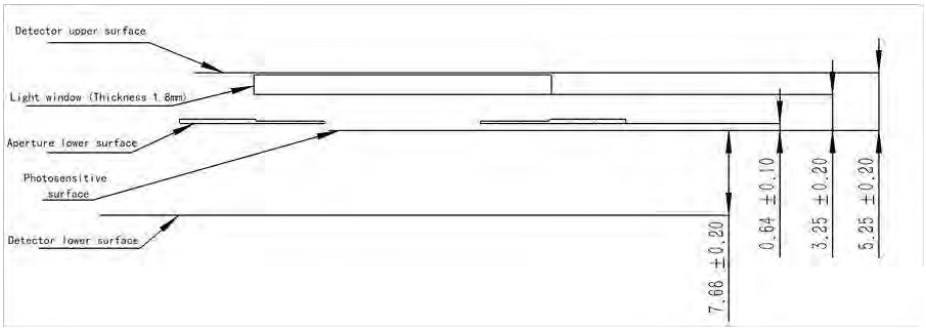
Optical Specification

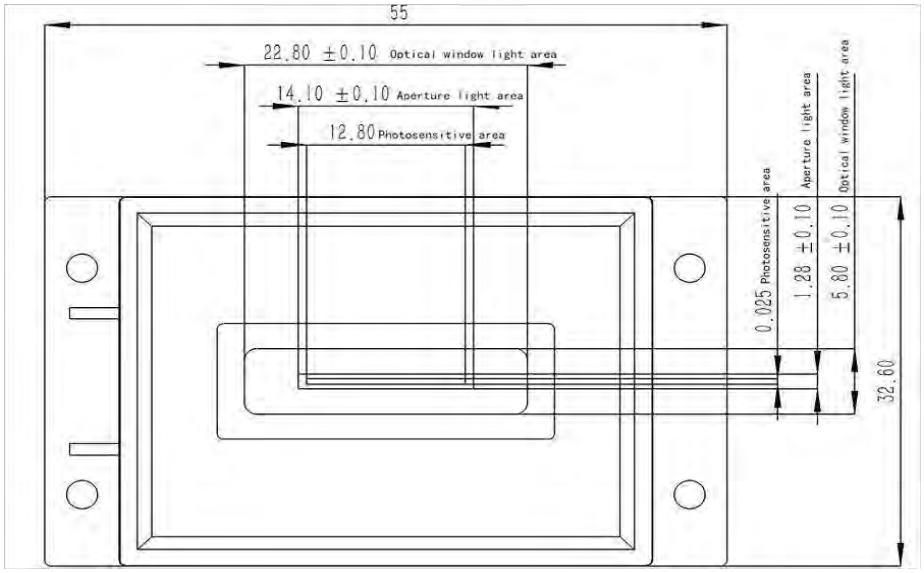
optical structure

This product uses a 512×1 element InGaAs focal plane, with 2 redundant elements on each end, that is, the total number of pixels is 516×1. In actual use, it is recommended to use the 3rd to 514th columns. The pixel shape is rectangular, the photosensitive size is 25μm×250μm, and the structure is arranged in a "one" shape, as shown in the figure below.

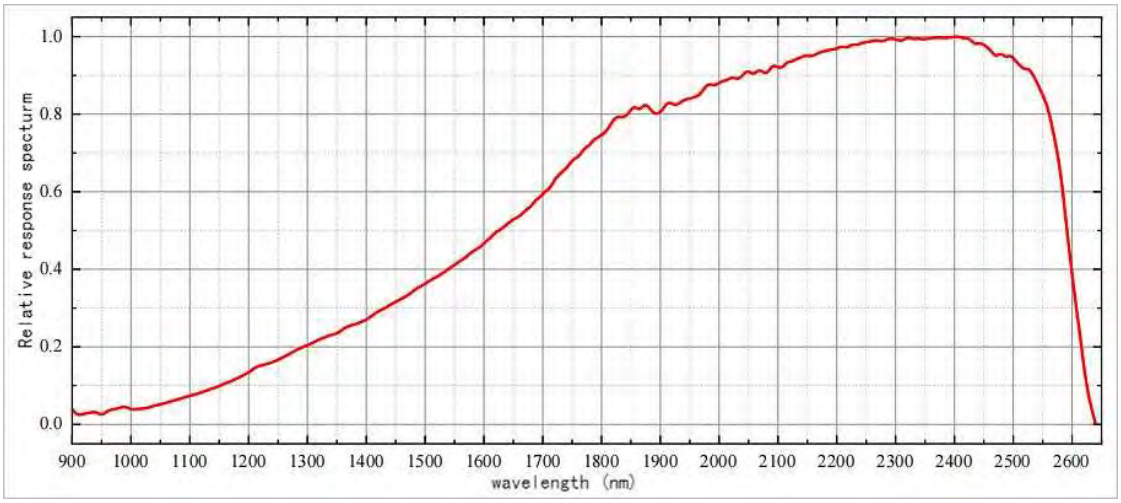


The optical window material is K9 glass with a thickness of 1.8mm and a transmittance of >90% in the response band. The center of the photosensitive surface is located at the center of the detector, with a relative position offset of ≤0.05mm and a relative rotation displacement of ≤0.02mm. The optical interface dimensions are shown in the figure below.



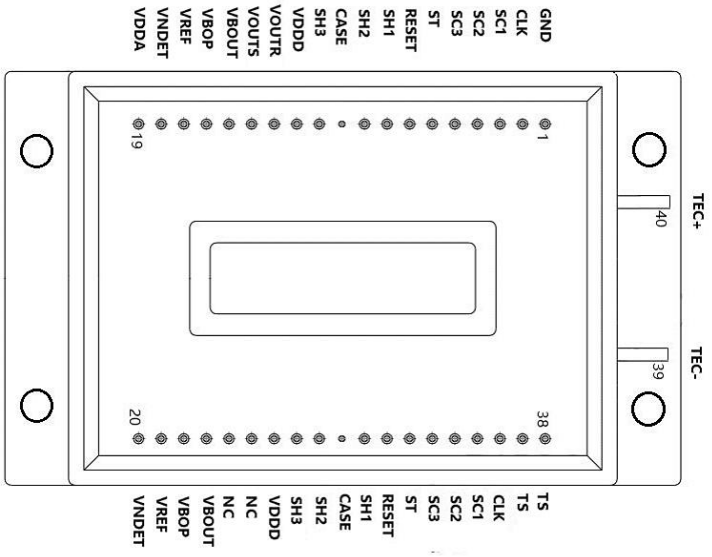


Relative Response Spectrum (Typical Value at Room Temperature)



Electrical Specification

Detector pin diagram



Pin Name	I/O	Function	Reference Value
GND	Input	Ground	Operating current<10mA
CLK	Input	Clock signal, provides timing reference for circuit driving	Digital voltage; High level 3.3V, Low level 0V
VDDD	Input	Digital circuit power supply, provides voltage for digital circuits inside the detector	DC 3.3V, operating current<5mA
VDDA	Input	Analog circuit power supply, provides voltage for analog circuits inside the detector	DC 3.3V, operating current<25mA
SC1, SC2, SC3	Input	Detector gain selection, controls detector output signal amplitude; see timing section	Digital voltage; High 3.3V, Low 0V
ST	Input	Trigger pulse, marks the start of circuit signal acquisition	Digital voltage; High 3.3V, Low 0V
RESET	Input	Reset signal, controls acquisition period duration; see timing section	Digital voltage; High 3.3V, Low 0V
SH1, SH2, SH3	Input	Sampling control signals, set integration time of pixels and change readout mode; see timing section	Digital voltage; High 3.3V, Low 0V
VBOUT	Input	Buffer bias voltage, provides bias to the circuit buffer	DC 2.3V

VBOP	Input	Amplifier bias voltage, provides bias to the signal amplifier	DC 2.3V~2.5V, recommended 2.4V
VREF	Input	Reference voltage, provides reference value for output signal	DC 2.3V
VNDET	Input	Detector chip common negative terminal	DC 2.3V
VOUTR	Output	Reference signal	0.5V~2.5V
VOUTS	Output	Output signal, calculated from reference signal minus output signal	0.5V~2.5V
TS	-	Temperature sensing resistor, measures resistance to calculate operating temperature	—
TEC+, TEC-	-	Thermoelectric cooler power supply; pin polarity as labeled	Do not exceed rated TEC voltage and current

Precautions

*Anti-static measures shall be taken during the transportation and use of the detector.

*Before powering on the detector, check the power connection status and drive settings. Strictly ensure that the operating current of each circuit does not exceed 60mA during power supply. Short-circuiting of the signal output terminal is prohibited, and it is recommended to supply power first, then apply the timing signal for operation.

*The DC input directly affects the overall noise of the detector; therefore, the following requirements are imposed on the ripple noise of the DC input power supply:

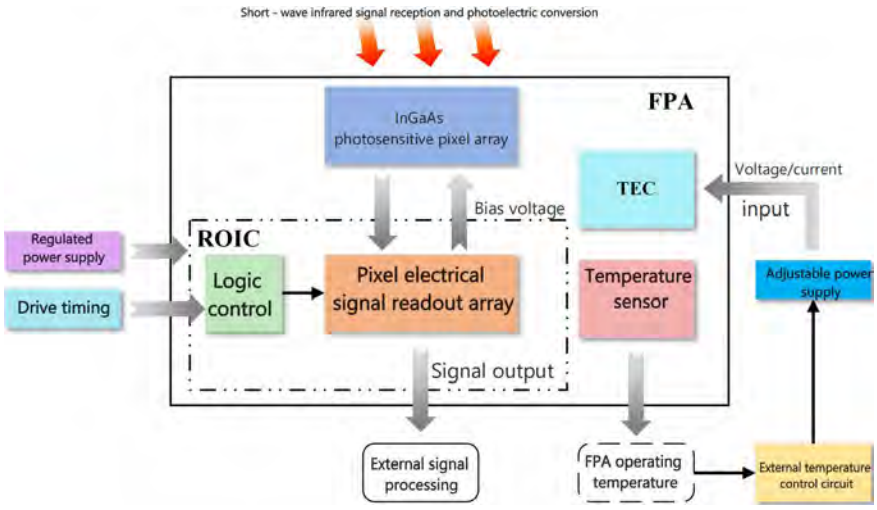
a) VDDA ＜ 2mV

b) VDDD ＜ 10mV

c) VREF, VNDET ＜ 0.3mV

d) VBOP, VBOUT ＜ 1mV

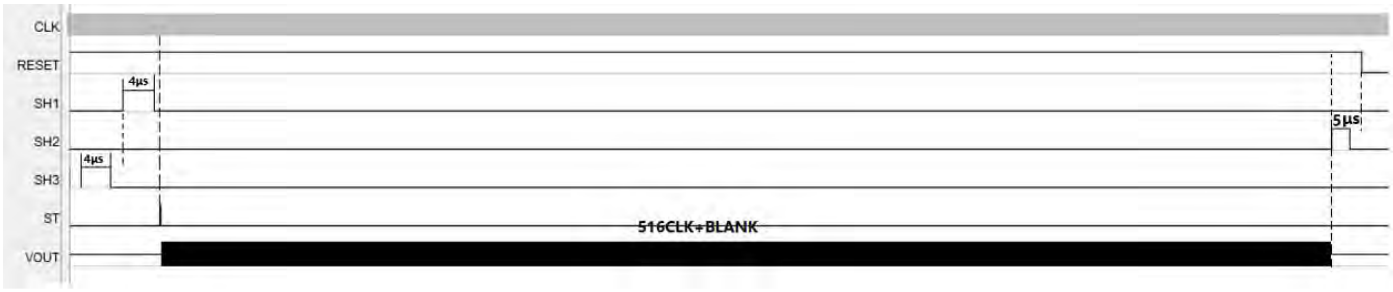
Diagram of Detector Working Principle and Connection Method



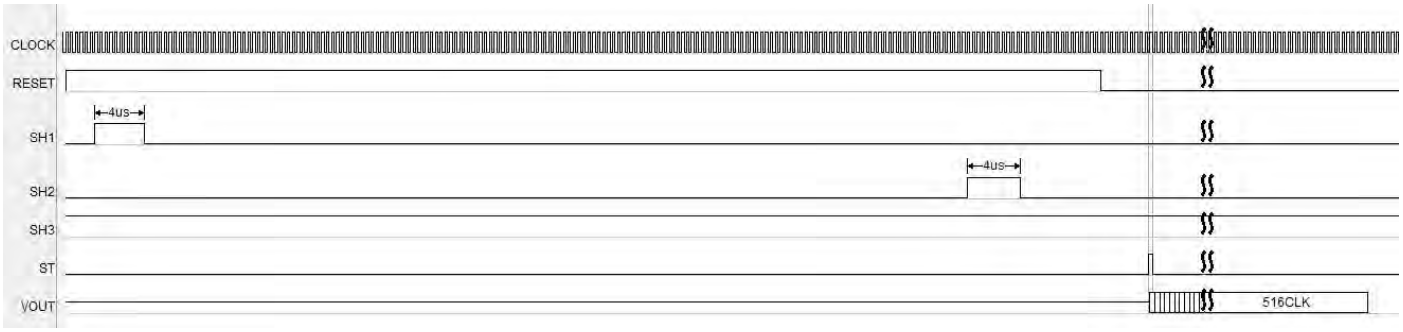
Detector Timing Description

The overall readout circuit driving timing pulse is shown in the following figure:

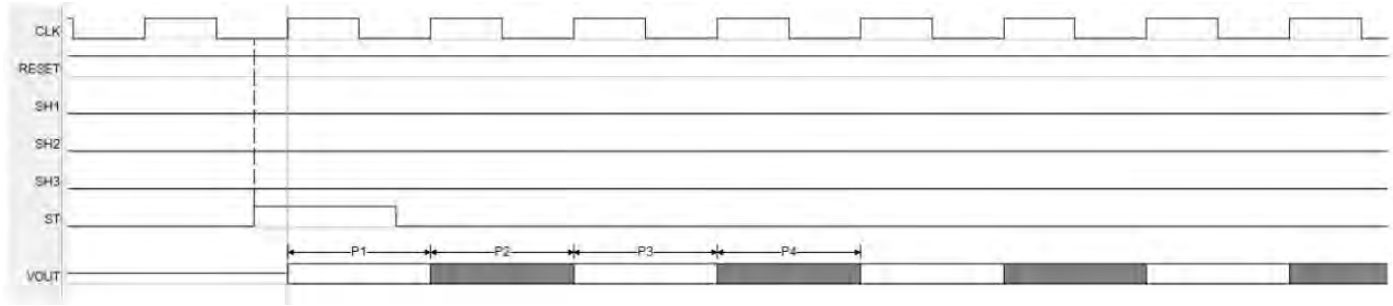
IWR mode:



ITR mode:



After zooming in, the timing details at the trigger level ST are as follows:



The overall timing requirements are as follows:

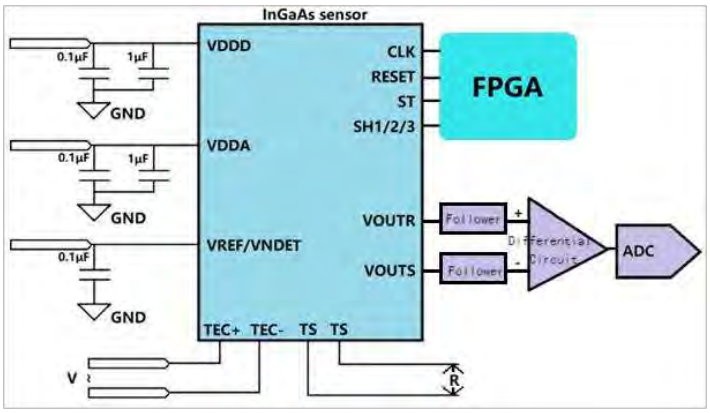
Name	High level width	Initial level	Rising edge time
CLK	0.5 CLK cycle	Low	0.5 CLK cycle
RESET	Adjust according to the integration time	High	
SH1		Low	6μs
SH2	4μs	Low	5μs before RESET falling edge
SH3	4μs	Low	1μs
ST	1 CLK cycle	Low	15μs

Precautions

*The CLK cycle and RESET high-level width can be set as required. The recommended frequency range for CLK is 1–10 MHz, and the RESET low-level width shall not be less than 2 μs.
*In IWR mode, the sequential positions of SH1, SH2, and SH3 must not be changed. The specific integration time of the detector is the time from the falling edge of SH1 to the falling edge of SH2 within the same RESET cycle.
*The ST high level needs to cover a complete CLK high level, and the rising edge of ST should be within the low level of CLK. It is recommended to set the rising edge at 1/2 of the CLK low level.
*The actual signal reading starts at the position of the first CLK rising edge after the ST rising edge, and the reference signal R and output signal S are read out in sequence until reaching the last CLK cycle before the falling edge of SH2.
*If the RESET high-level width is insufficient to read out all 516 pixels, when the next RESET high level arrives, reading still starts from the first pixel instead of from the unread pixels. If the RESET high-level width is too large, after reading all 516 pixels of the channel, empty sampling will continue until the RESET low level arrives for reset.
*For SC1, SC2, and SC3, it is recommended to use digital input voltage, that is, always maintain 3.3V high level / 0V low level.
This detector features 8 gain levels, and the lowest gain level (Level 8) is recommended for use. The specific relationship between gain levels and input voltage is shown in the table below:

Gain Levels	SC1	SC2	SC3	Gain
1	1	1	1	High
2	0	0	0	
3	0	0	1	
4	0	1	0	
5	0	1	1	
6	1	0	0	
7	1	0	1	
8	1	1	0	Low

Detector peripheral recommended circuit diagram



Thermal Parameters

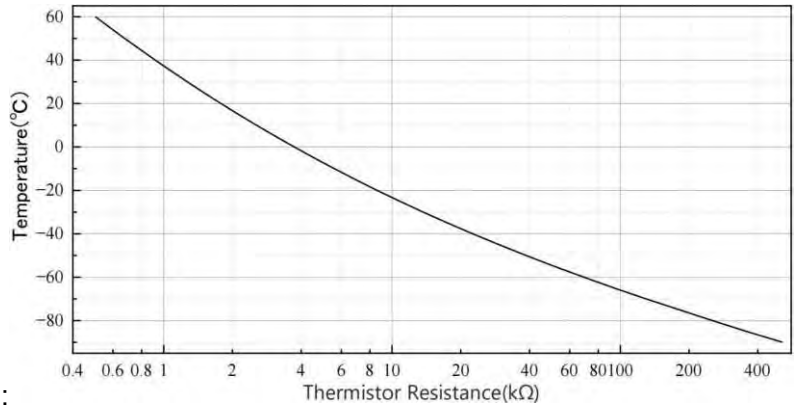
The detector integrates a two-stage thermoelectric cooler (TEC). The center of the heat dissipation surface is aligned with the center of the detector's lower surface, and the heat dissipation area shall be ≥ 20mm × 20mm. Its performance parameters are shown in the table below:

Performance Indicator	Value
Maximum Temperature Difference Between Cold and Hot Sides ($\triangle T_{max}$/°C) *	45
Maximum Allowable Load Current ($I_{teC\text{-}max}$/A)	2.72
Maximum Allowable Load Voltage ($V_{teC\text{-}max}$/V)	13.5

*This performance indicator specifically refers to the temperature difference between the focal plane and the heat dissipation surface of the package structure.

Characteristics of the Temperature Sensor

This product uses a thermistor as the temperature sensor. Within the operating temperature range, the corresponding relationship between the thermistor's resistance value and temperature is shown in the figure below



:

Typical Corresponding Relationship Between Thermistor Resistance and Temperature

Temp.(℃)	Res.(kΩ)	Temp.(℃)	Res.(kΩ)	Temp.(℃)	Res.(kΩ)	Temp.(℃)	Res.(kΩ)	Temp.(℃)	Res.(kΩ)
-50	38.7	-30	13.69	-10	5.587	10	2.55	30	1.268
-45	29.4	-25	10.81	-5	4.549	15	2.126	35	1.077
-40	22.56	-20	8.608	0	3.729	20	1.782	40	0.918
-35	17.49	-15	6.909	5	3.075	25	1.5	45	0.786

Corresponding Relationship Between Thermistor Resistance and Temperature (Expressed by the Following Formula):

$$\frac{1}{(T_1+273.15)}=\frac{\ln\left(\frac{R_1}{R_2}\right)}{B}+\frac{1}{(T_2+273.15)}$$

T1: Test target temperature, Unit: ℃

T2: Reference point temperature, Unit: ℃. Within the range of -70~30℃, the typical values of reference temperature are -40℃ or -10℃, and a reference temperature value close to the target temperature should be selected.

R1, R2: Thermistor resistance values corresponding to T1 and T2 respectively, Unit: kΩ

B: Thermistor coefficient. Within the range of -70~30℃, the typical value of B-40/-10 is 2854.43 (with a deviation of ±2%), and the temperature deviation calculated from this typical value is ±0.5℃.

Notes

a) During the installation of the TEC, attention should be paid to the additional resistance introduced by the external electrical structure. If the additional resistance exceeds 10% of the TEC resistance, the I-V curve must be recalibrated.

b) It is recommended to connect the TEC in a way that minimizes the connection resistance. If pin soldering is necessary, short-circuit grounding protection should be implemented. The local temperature during pin soldering must be ≤ 250℃, and the soldering duration must be < 10s.

c) If higher measurement accuracy is required within a small temperature range, the B-value can be calculated independently as needed.

d) Before turning on the TEC, it is mandatory to confirm the following: the temperature sensor is working normally, the heat dissipation surface is in full contact with the heat sink, the heat dissipation surface meets the required

size, and the heat sink is functioning properly. It is not recommended to turn on the TEC without installing the heat sink or when the heat sink is not working.

e) When turning on the TEC for the first time, the current or voltage should be gradually applied starting from 0A or 0V. Meanwhile, monitor the temperature change until the preset temperature is reached.

f) Since the detector performance is affected by temperature, the TEC should be turned on first and stabilized at the target temperature before activating the detector. It is not recommended to operate the detector in an environment with fluctuating temperatures.

g) When the detector is not in use for an extended period, power supply to the TEC should be stopped to extend the TEC's service life.

h) The cooling effect of the detector is related to the ambient temperature, power supply performance, and heat dissipation status. It is recommended to properly match the heat dissipation system according to the actual operating environment and the required detector performance.

Product Support

Issue	Possible Causes	Solutions
Abnormal Signal Output of Detector	No power supply or abnormal power supply	Check if each power supply meets the electrical requirements specified in the manual.
	Abnormal timing	Adjust the detector's timing pulse width according to the recommended values in the manual.
	Short integration time or no light intensity	Increase the integration time and switch the gain level.
	Light intensity saturation	Shorten the integration time and switch the gain level.
Excessive Output	High ripple noise of power supply	Supply power in accordance with the electrical requirements for DC power supply ripple noise in the manual.
	Reverse connection of TEC pins	Determine whether reverse connection exists by detecting with a temperature sensor.
Noise of Detector	Noise introduction from backend electronic circuits	Inspect the layout of the board-level circuit structure and the status of circuit noise.