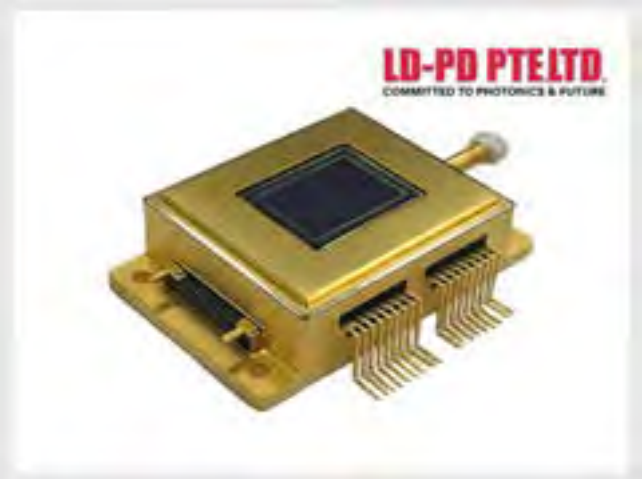
640×512 InGaAs Area Array Detector



Description

The LP6515V3-A type InGaAs area array detector is mainly composed of a 640×512-scale InGaAs photosensitive chip, a readout integrated circuit (ROIC), and a three-stage thermoelectric cooler (TEC). It adopts a metal vacuum packaging form and features wavelength extension, window-openable function, and high frame rate detection. It can be applied in fields such as short-wave infrared imaging and spectral detection.

Specifications

Main optoelectronic specifications

Parameter	Typical Value
Spectral Response Range (μm)*1	1.00 ±0.05 ~ 1.90 ±0.05
Effective Pixel Rate (%)*2.3	≥99
Noise Electrons (e^-)*3	≤300
Dark Current Density (nA/cm²)*1	≤10
Dynamic Range (dB)*1	≥50 (MG)
Voltage Conversion Gain (μV/e^-)	0.9 (LG), 20 (MG), 90 (HG)
Voltage Output Swing (V)	1.8
Response Non-uniformity (%)*3	≤8
Peak Quantum Efficiency (%)	≥60
Readout Modes	IWR, ITR, CDS, IMRO, NDRO
Number of Output Channels	2, 4, 8

Readout Rate (MHz)	2 ~ 18
Maximum Full-frame Output Frame Rate (Hz)	300

*1 Focal Plane Chip Temperature = -20℃

*2 Under the condition near the optical signal half-well, the percentage of pixels where the deviation between the response signal and the average value is less than 50%

*3 Chip Temperature = -20℃, MG Gain, Integration Time 2ms, IWR Mode

The above data were obtained without enabling the CDS mode during testing

Mechanical Parameter

Parameter	Typical Value
Length × Width × Height (mm³)	60 × 44 × 11.55
Weight (g)	~60
Focal Plane Array Size	640 × 512
Pixel Pitch (μm)	15
Pixel Size (μm²)	15 × 15
Photosensitive Area (mm²)	9.6 × 7.68

Operating Environment & Power Consumption Spec

Parameter	Typical Value
Operating Temperature (°C)	-20 ~ +60
Storage Temperature (°C)	-40 ~ +70
Typical Power Consumption (W)	<0.5

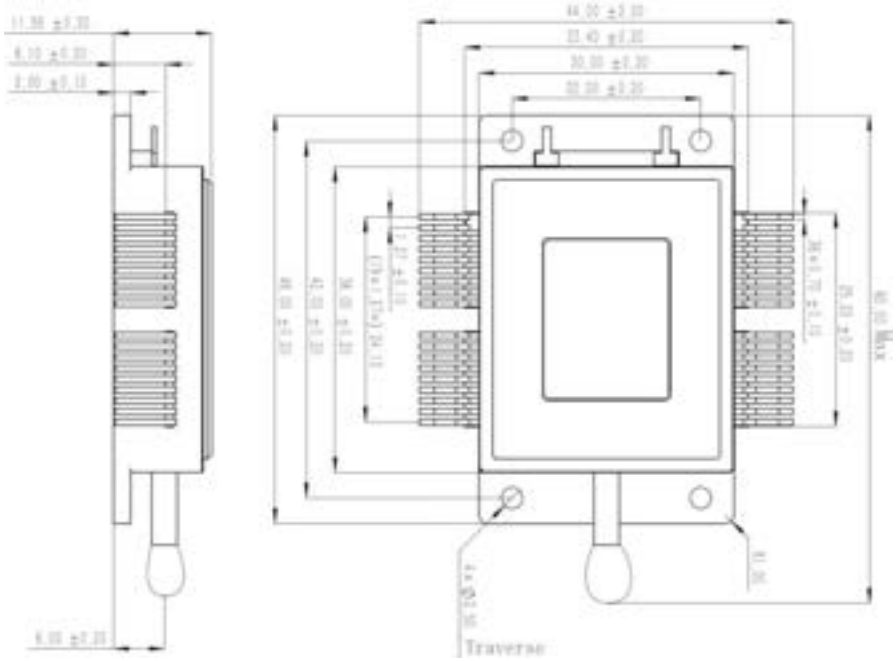
TEC Disabled, Ambient Temperature = 25℃, Number of Readout Channels = 8, Power Consumption Control Gear = 100%

Mechanical Specification

This InGaAs area array detector adopts a metal package with vacuum sealing. The metal shell is made of FeNiCoSi alloy, with a Ni/Au electroplated layer on the surface. The window is bonded via In-based brazing, and the cover is sealed by resistance welding. The external dimensions of the detector are 60mm (Length) x 44mm (Width) x 11.55mm (Height).

Thirty-six pins (0.7mm x 0.25mm) are led out from the side of the shell, arranged in a single-row "linear" pattern on both sides. The spacing between adjacent pins on one side is 1.27mm. These pins are used for the input of focal plane power supply and commands, the input of thermoelectric cooler (TEC) power supply, and the electrical lead-out of focal plane detection signals and temperature sensor signals. Additionally, two pins (1.0mm

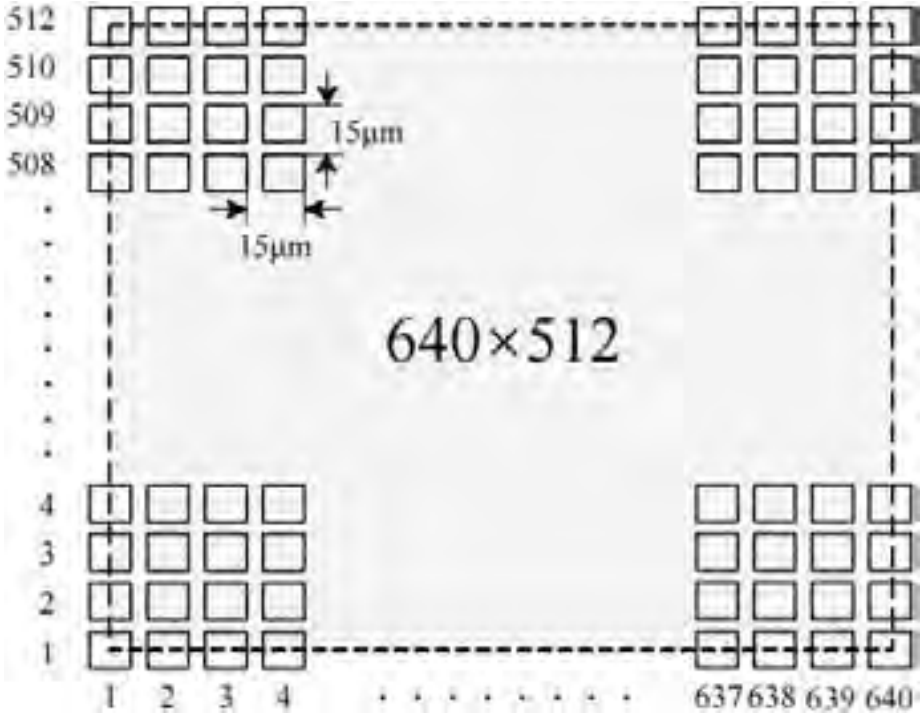
x 0.5mm) on the side are used for getter activation. Four through-holes (Φ2.5mm) are distributed on both sides of the package for detector fixation.



Optical Specification

optical structure

This detector adopts a 640×512-pixel InGaAs focal plane array, with a pixel pitch of 15 μm. The pixels are square-shaped, and each photosensitive pixel has a size of 15 μm × 15 μm.

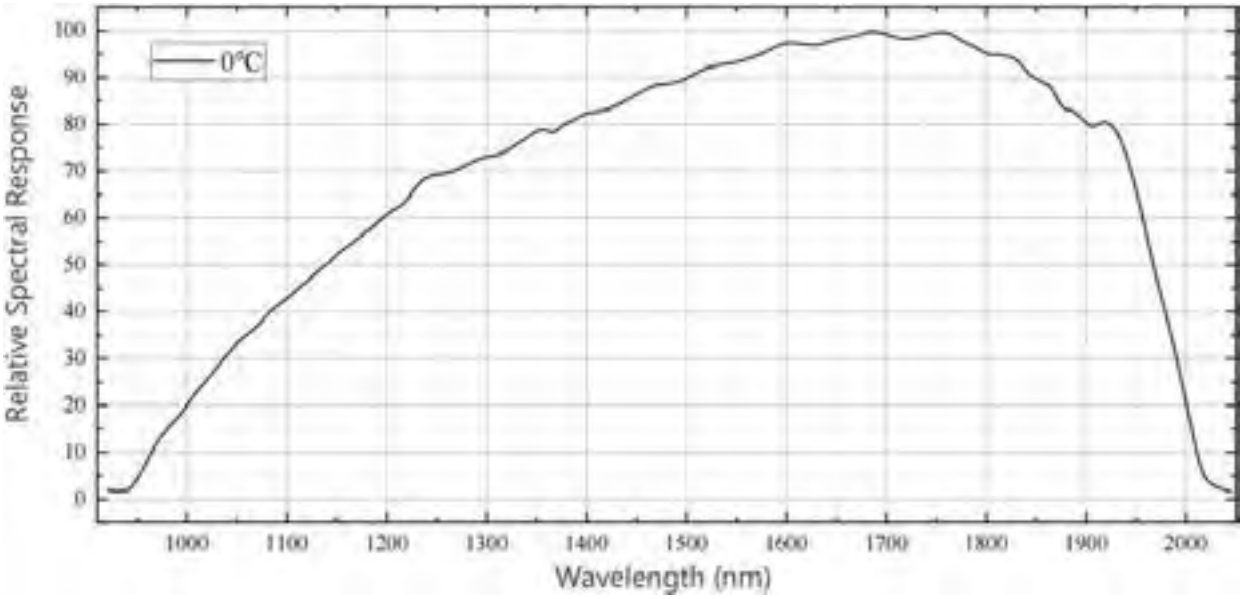


This detector features a designed distance of 3.4 mm between its photosensitive surface and the upper surface of the package structure, 2.45 mm between its photosensitive surface and the lower surface of the optical window, and 1.05 mm between its photosensitive surface and the lower surface of the diaphragm.

The optical window is made of sapphire, with a thickness of 0.9 mm and a refractive index of 1.76. Its surface is coated with an anti-reflective (AR) coating, ensuring a transmittance of >95% within the response wavelength range. The light-transmitting area of the optical window measures 15 mm × 11 mm, while the light-transmitting size of the diaphragm is 10.2 mm × 8.2 mm.

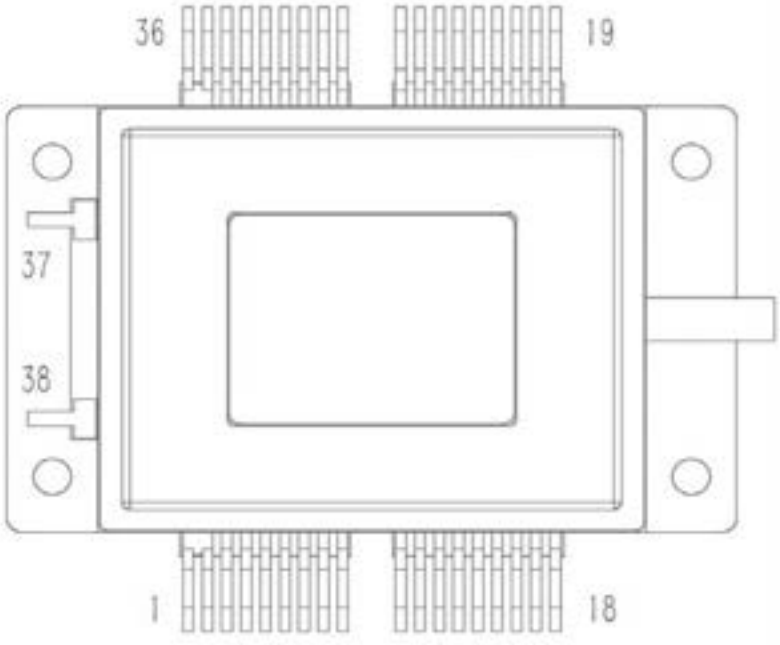
The center of the photosensitive surface is aligned with the center of the detector, with a relative positional deviation of ≤0.05 mm and a relative rotational displacement of ≤0.02 mm.

Relative Spectral Response (Typical Value)



Electrical Specification

Pin Defination



Pin Number	Pin Name	Input/Output	Pin Function	Reference Value
1-2	TEC+	-	Connection pin + for thermoelectric cooler, cannot be reversed	-
3	NC	-	No connection, empty pin	Must be floating
4	RESET	Input	External reset input (active high)	-
5	SERIAL	Input	Serial command word input	Digital voltage, high level 3.3V, low level 0V
6	ST	Output	Frame output identifier	-
7	ROW_ST	Output	Row output identifier	-
8	NC	-	Same as pin 3	-
9-10	TS1	-	Temperature sensor, measure resistance value through two pins to feedback the operating temperature of the focal plane	-
11/12	VOUT1/2	Output	The first/second channel in eight - channel, four - channel and two - channel output modes	-

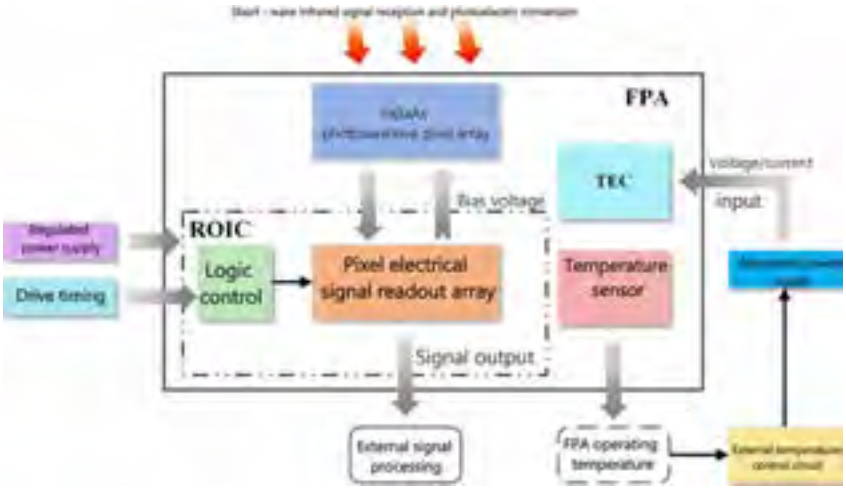
13/14	VOUT3/4	Output	The third/fourth channel in eight - channel and four - channel output modes	-
15~18	VOUT5 - 8	Output	The fifth/sixth/seventh/eighth channel in eight - channel output mode	-
19	VDDA2	Input	Analog power supply	3.3 - 3.8V, typical 3.6V, drive current > 150mA
20	VDDA1	Input	Analog IO power supply	3.3 - 3.8V, typical 3.6V, drive current > 80mA
21	GNDA1	-	Analog power ground	-
22	GNDA2	-	Analog power ground	-
23	SUBPV*	Input	Common N - terminal of detector	2.7 - 3.2V, drive current > 5mA
24	VBLM	Input	Bias voltage, generated internally, supports external adjustment	0 - 2.0V, typical 1.0V, drive current > 5mA
25	VREF	Input	Bias voltage input	3.0 - 3.3V, typical 3.3V, drive current > 60mA
26/27	TS2	-	Same as pin 9/10	-
28	VD33	Input	Digital IO power supply	3.0 - 3.3V, typical 3.3V, drive current > 20mA
29	GNDD	-	Digital ground	-
30	VD18	Input	Digital logic power supply	1.62 - 1.98V, typical 1.8V, drive current > 30mA
31	NC	-	Same as pin 3	-
32	INT	Input	Integration control input	Digital voltage, high level 3.3V, low level 0V
33	CLK	Input	Detector main clock	Digital voltage, high level 3.3V, low level 0V
34	NC	-	Same as pin 3	-
35/36	TEC-	-	Connection pin - for thermoelectric cooler, cannot be reversed	-
37/38	Getter	-	Getter activation pin	Must be floating

*It is recommended that the supply voltage be adjusted according to the focal plane temperature: 2.88V@RT, 2.86V@0℃, 2.84V@-20℃

Precautions:

The DC input directly affects the overall noise of the detector. Therefore, there are the following requirements for the ripple noise of the DC input power supply:
Ripple noise requirements for each power supply voltage:
a) VDDA1: < 1mV;
b) VDDA2: < 10mV;
c) VD33: < 10mV;
d) VD18: < 10mV;
Load requirements for signal output terminals (VOUT1 - VOUT8): Cload < 25pF; Rload > 100kΩ;
Range of logic output signals (ROW_ST, ST): The logic output signals are high - and low - level digital signals, where
a) Low level: 0 - 0.3V;
b) High level: (VD18 - 0.3V) - VD18;
c) Load requirements for logic output terminals: Cload < 15pF

Diagram of Detector Working Principle and Connection Method



Detector Timing Description

ITR Mode

The schematic diagram of the readout circuit driving timing pulses is as follows.

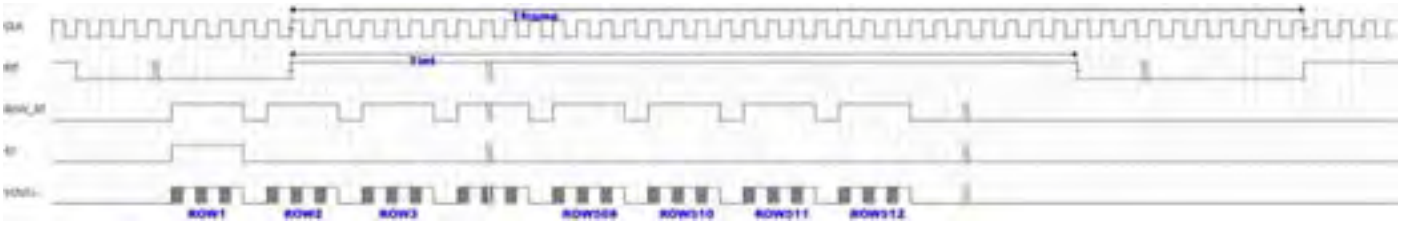


Timing Details:

a) The serial port command word input must be completed before the start of integration;
b) INT, as the integration time control signal, has both high and low level durations equal to an integer number of Tclk;
c) After the completion of the current frame integration Tint, a period of Thold (93 Tclk) is required before starting the readout of the integration signal. During the readout process of the current frame signal, the readout starts row by row from the first row. After each row is read out, a period of Td (32 Tclk) is required before starting the readout of the integration signal of the next row, until all signal readouts are completed;
d) When the readout of the current frame integration signal starts, the detector synchronously outputs ST and ROW_ST voltage signals, where ST is the frame output flag; ROW_ST is the row output flag, and a high level indicates that the signal is being read out. The high level width is Tclk × C/N, where C is the number of columns and N is the number of output channels. The interval between adjacent high levels is Td until the readout of the integration signal is completed;
e) In each output channel, reading out the integration signal of one pixel requires one main clock Tclk. The readout time Tout = C × R/N × Tclk + (R-1) × Td, where R is the number of rows; the working frame period $T_{frame} = T_{int} + T_{hold} + T_{out}$.

IWR Mode

The schematic diagram of the readout circuit driving timing pulses is as follows.



Timing Details:

a) The serial port command word input must be completed before the start of integration;
b) In this mode, the integration of the pixel signal of the current frame and the readout of the integration signal of the previous frame are completed simultaneously within one frame period;
c) INT, as the integration time control signal, has both high and low level durations equal to an integer number of Tclk, and the low level width of INT must be greater than 45 Tclk;
d) After the completion of the current frame integration Tint, a period of Thold (93 Tclk) is required before starting the readout of the integration signal. During the signal readout process, the readout starts row by row from the first row. After each row is read out, a period of Td (32 Tclk) is required before starting the readout of the integration signal of the next row, until all signal readouts are completed;
e) When the readout of the current frame integration signal starts, the detector synchronously outputs ST and ROW_ST voltage signals, where ST is the frame output flag; ROW_ST is the row output flag, and a high level

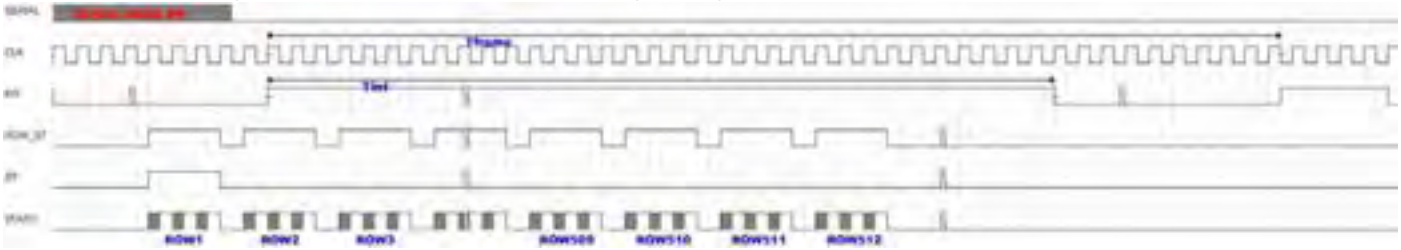
indicates that the signal is being read out. The high level width is Tclk × C/N, and the interval between adjacent high levels is Td until the readout of the integration signal is completed;

f) In each output channel, reading out the integration signal of one pixel requires one main clock Tclk. The readout time Tout = C × R/N × Tclk + (R-1) × Td;

g) The frame period is approximately equal to the readout time, and the overall frame period: Tframe ≥ Thold + Tout + 320Tclk.

NDRO Mode

The schematic diagram of the readout circuit driving timing pulses is as follows:



Timing Details:

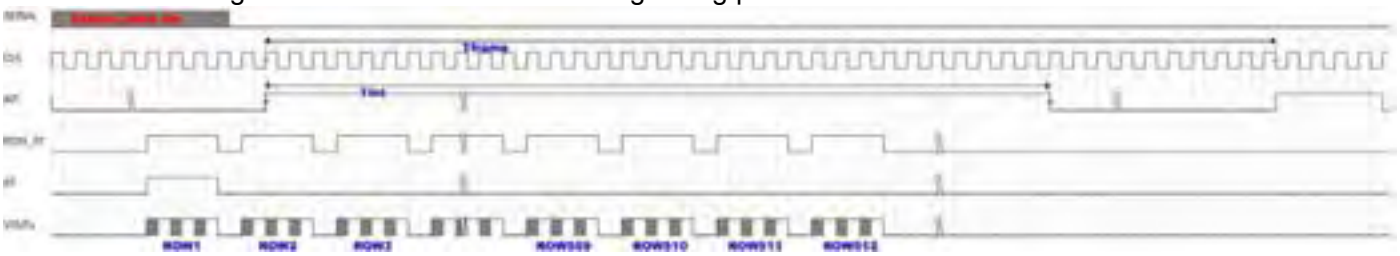
a) In the serial port command word configuration, after setting the coding bit that controls NDRO readout to enable the NDRO mode, the detector continues to perform integration according to the IWR readout mode, but does not conduct signal sampling;

b) The output signal value remains the integration signal of the last frame before entering the NDRO mode, and the held signal of this frame is output in a repeated cycle;

c) After setting the coding bit that controls NDRO readout to disable the NDRO mode, the detector enters the IWR readout mode. However, the held signal is still output in this frame, and the normal IWR integration signal is output in the next frame.

IMRO Mode

The schematic diagram of the readout circuit driving timing pulses is as follows:



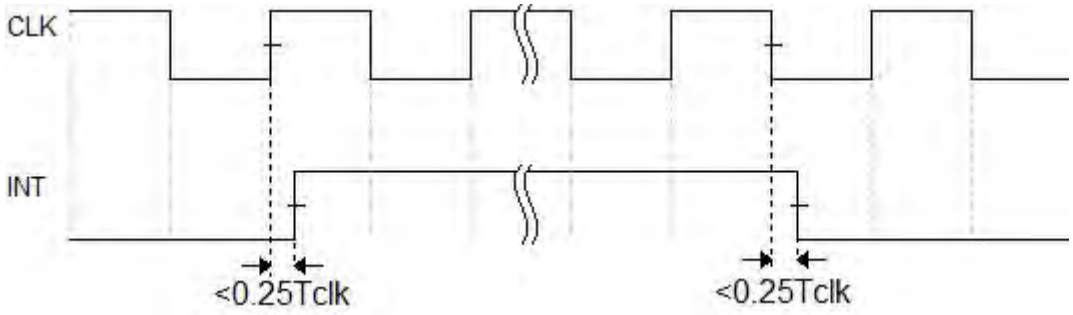
Timing Details:

a) In the serial port command word configuration, after setting the coding bit that controls IMRO readout to enable the IMRO mode, the detector continues to perform signal sampling according to the IWR mode, but the

integration proceeds continuously, and the output signal value is the result of integration within the previous Tframe;

b) After modifying the command word to disable the IMRO mode, the detector enters the IWR readout mode.

Notes: The input clock CLK and the rising/falling edges of INT must satisfy a certain relationship. Both the rising edge and falling edge of INT should lag behind the falling edge of CLK (typically by 10ns), but the delay time must not exceed 0.25 times the time width of the main clock CLK.



Serial Port Command Word Configuration

Definition of Each Bit of the Command Word

Data No.	Name	Function	Length	Recommended Value (1/0 for high/low level respectively)
1 - 4	Start[3:0]	Serial port enable control	4bit	4'b1101
5 - 6	Gain[1:0]	Integration gain control	2bit	2'b00
7	UPcol	Image flip control	1bit	1'b1
8	UProw	Image flip control	1bit	1'b1
9	SizeA	Window format	1bit	1'b1
10	SizeB	Window format	1bit	1'b1
11 - 19	Cstart[8:0]	Custom window control: window	9bit	9'b0

		start row and column coordinates		
20 - 28	Cfinal[8:0]	Custom window control: window start row and column coordinates	9bit	9'b0
29 - 37	Rstart[8:0]	Custom window control: window start row and column coordinates	9bit	9'b0
38 - 46	Rfinal[8:0]	Custom window control: window start row and column coordinates	9bit	9'b0
47 - 48	Pctrl[1:0]	Global power consumption control	2bit	2'b01
49 - 50	NBOUT[1:0]	Output channel number control	2bit	2'b11
51 - 53	Ppix[2:0]	Pixel power consumption control bit	3bit	3'b010
54 - 55	Pbuf[1:0]	Column BUF power consumption control	2bit	2'b01
56 - 57	Pfo[1:0]	Drive signal setup time control	2bit	2'b01
58	Pout	Output BUF	1bit	1'b0

		power consumption control		
59 - 61	Tpre[2:0]	Integration preparation time control	3bit	3'b101
62	BLM_EN	Anti - blooming enable control	1bit	1'b1
63 - 65	BLM_CTL[2:0]	Anti - blooming voltage configuration	3bit	3'b010
66	TEST1	Test mode control bit 1	1bit	1'b0
67 - 70	TEST2[3:0]	Test mode control bit 2	4bit	4'b1011
71 - 74	Tcds[3:0]	CDS sampling time control	4bit	4'b0111
75	TEST3	Test mode control 3	1bit	1'b0
76	CDS_MODE	CDS mode control	1bit	1'b1
77	NDRO	NDRO mode control	1bit	1'b0
78	IMRO	IMRO mode control	1bit	1'b0
79	OUTbw	Bandwidth limitation control	1bit	1'b1
80 - 103	TEST4[23:0]	Test mode control bit 4	24bit	24'b 0010 0000 0000 0000 0000 0000

Gain [1:0] - Gain Level Control

Gain[1]	Gain[0]	Corresponding Gain
0	0	HG (default)
0	1	MG
1	x	LG

Control Mode

IMRO	NDRO	Gain[1]	CDS_MOD	Readout Mode
0	0	0	1	CDS Mode (Default)
0	0	0	0	Non-CDS Mode
0	0	1	x	Non-CDS Mode
0	1	0	0	NDRO Mode (Under Non-CDS Mode)
0	1	0	1	NDRO Mode (Under CDS Mode)
0	1	1	x	NDRO Mode (Under Non-CDS Mode)
1	x	0	0	IMRO Mode (Under Non-CDS Mode)
1	x	0	1	IMRO Mode (Under CDS Mode)
1	x	1	x	IMRO Mode (Under Non-CDS Mode)

Notes

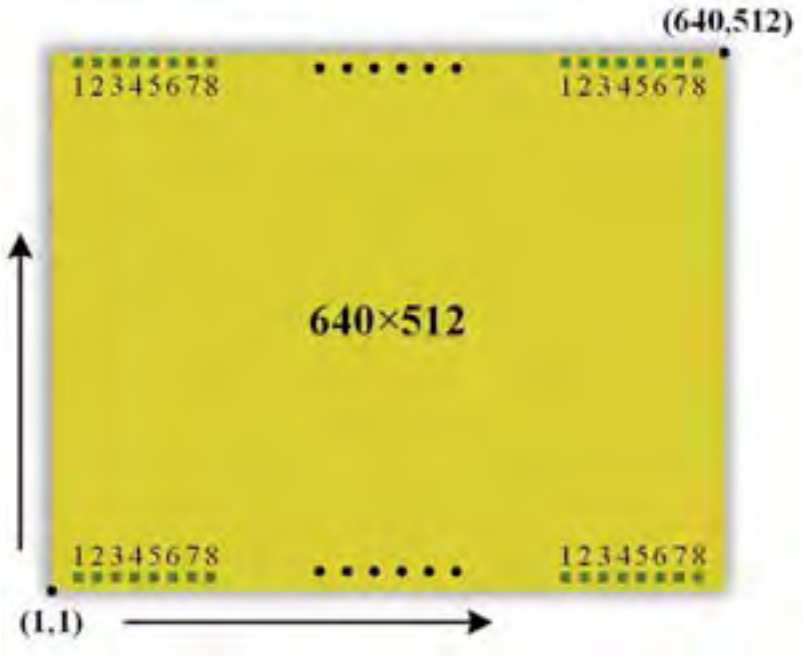
a) The IMRO mode is controlled by the IMRO (Multiple Integration Readout) command word; the NDRO mode is controlled by the NDRO (Non-Destructive Readout) command word; the CDS mode is controlled by the CDS_MODE command word;
b) The priority order of each command word is IMRO > NDRO > CDS_MODE, and Gain[1] > CDS_MODE;
c) During the process of switching from "CDS mode" to "Non-CDS mode", it is recommended to first switch to "Non-CDS Low Gain Mode", and then switch to "Normal Non-CDS Operating Mode".

Image Flip Control: UPCOL, UPROW

When the TEC pins are oriented to the left, the default origin (1, 1) is at the bottom-left corner, and the readout proceeds toward the top-right corner (640, 512);

UPcol	UProw	Image Output Order
1	1	Top-right starting point, right to left, top to bottom (Default)

1	0	Bottom-right starting point, right to left, bottom to top
0	1	Top-left starting point, left to right, top to bottom
0	0	Bottom-left starting point, left to right, bottom to top



*Note: The above diagram is a schematic of the readout sequence when the TEC pins are oriented to the left and 8-channel readout is enabled.

Preset Window Size Control: SizeA, SizeB

SizeA	SizeB	Window Size
1	1	Full Frame 640×512 (Default)
1	0	Central Area 640×480
0	1	Central Area 512×512
0	0	Custom Size

Custom Window Setting

a) The number of window rows is independent of the number of output channels.
Starting row: 0 ≤ Rstart ≤ 508
Ending row: 0 ≤ Rfinal ≤ 511
b) 2-channel output (NBOUT[1:0] = 2'b00 or 2'b01):
Starting column: 2 × Cstart, where 0 ≤ Cstart ≤ 318
Ending column: 2 × Cfinal + 1, where Cstart + 1 ≤ Cfinal ≤ 319
Minimum window size: 4 (rows, R) × 4 (columns, C)

c) 4-channel output (NBOUT[1:0] = 2'b10):
Starting column: 4 × Cstart, where 0 ≤ Cstart ≤ 158
Ending column: 4 × Cfinal + 3, where Cstart + 1 ≤ Cfinal ≤ 159
Minimum window size: 4 (rows, R) × 8 (columns, C)
d) 8-channel output (NBOUT[1:0] = 2'b11):
Starting column: 8 × Cstart, where 0 ≤ Cstart ≤ 78
Ending column: 8 × Cfinal + 7, where Cstart + 1 ≤ Cfinal ≤ 79
Minimum window size: 4 (rows, R) × 16 (columns, C)

Power Consumption Control: Pctrl [1:0]

Pctrl [1]	Pctrl [0]	Power Consumption Ratio
1	1	200%
1	0	150%
0	1	100% (Default)
0	0	50%

Number of Output Channels: NBOUT[1:0]

NBOUT[1]	NBOUT[0]	Status
0	x	2 Channels
1	0	4 Channels
1	1	8 Channels (Default)

Pixel Power Consumption Control: Ppix [2:0]

Ppix [2]	Ppix [1]	Ppix [0]	Pixel Power Consumption
0	0	0	33%
0	0	1	67%
0	1	0	100% (Default)
0	1	1	133%
1	0	0	167%
1	0	1	200%
1	1	0	233%
1	1	1	267%

Column BUF Power Consumption Control: Pbuf[1:0]

Pbuf[1]	Pbuf[0]	Power Consumption Ratio
1	1	200%
1	0	150%
0	1	100% (Default)
0	0	50%

Driver Signal Setup Time Control: Pfol [1:0]

Pfol [1]	Pfol [0]	Control Signal Rise/Fall Time
0	0	1.5μs
0	1	0.8μs (Default)
1	0	0.5μs
1	1	<350ns

Output BUF Power Consumption Control: Pout

Pout	Power Consumption Ratio
1	131%
0	100%(Default)

Integration Preparation Time Control: Tpre [2:0]

The INT high-level width (i.e., integration time) must be longer than the integration preparation time. To achieve the shortest integration time, the configuration of Tpre [2:0] should be set to 3b'111.
In CDS mode (Correlated Double Sampling mode), the integration time must be longer than the sum of the Tpre [2:0] time and the Tcds time.

Tpre [2]	Tpre [1]	Tpre [0]	Integration Preparation Time
0	0	0	100μs
0	0	1	50μs
0	1	0	20μs
0	1	1	4μs
1	0	0	2μs
1	0	1	1μs（Default）
1	1	0	0.5μs
1	1	1	120ns

Anti-blooming Function Control BLM_EN and BLM_CTL [2:0]

BLM_EN	BLM_CTL[2:0]	VL Voltage Value
0	X	0V
1	000	0.80V
1	001	0.93V
1	010	1.00V (Default)
1	011	1.07V
1	100	1.15V
1	101	1.21V
1	110	1.28V
1	111	1.35V

Tcds Clock Count Control Signal: Tcds

In CDS mode (Correlated Double Sampling mode), the integration time must be longer than the time configuration of T_{CDS}.

Tcds	Tcds Clock Count	Tcds	Tcds Clock Count
0000	0Tclk	1000	540Tclk
0001	36Tclk	1001	612Tclk
0010	108Tclk	1010	684Tclk
0011	180Tclk	1011	756Tclk
0100	252Tclk	1100	828Tclk
0101	324Tclk	1101	900Tclk
0110	396Tclk	1110	972Tclk
0111	468Tclk (Default)	1111	1044Tclk

Bandwidth Limitation Control: OUTbw

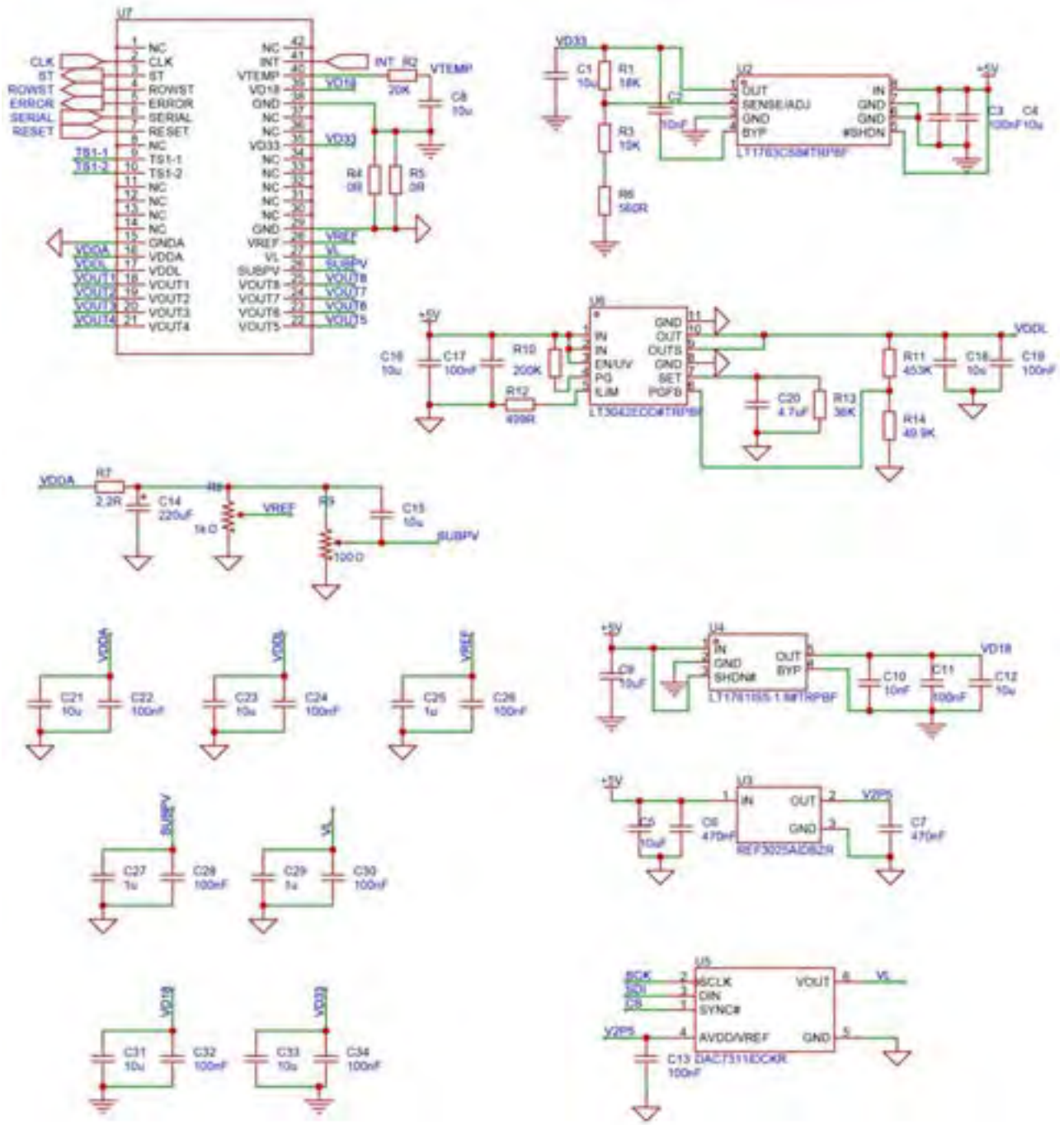
OUTbw	Bandwidth Limitation Function
0	No Limitation
1	Bandwidth Limitation (Default)

Configuration Method for Short Integration Applications

When CDS_MODE = 1'b0 (non-CDS mode) and Tpre = 3'b111 are set simultaneously, the circuit enters non-CDS mode. In this mode, the circuit supports configurations where the minimum integration time is longer than 3Tclk.

This configuration is suitable for application scenarios requiring short exposure times, such as active illumination gated imaging.

Recommended Peripheral Circuit Diagram for Detector



Thermal Parameters

Thermoelectric Cooler (TEC) Characteristics

A 3-stage thermoelectric cooler (TEC) is integrated into the detector. The center of the heat dissipation surface aligns with the center of the detector's lower surface, and the heat dissipation area must be ≥ 36mm × 30mm. Its performance parameters are shown in the table below:

Performance Indicator	Value
Maximum Temperature Difference Between Hot and Cold Surfaces (△Tmax/℃) *	70
Maximum Allowable Operating Current (ITEC-max/A)	3.6
Maximum Allowable Operating Voltage (VTEC-max/V)	6.2
AC Impedance (Including AC Resistance) (ACR/Ω)	1.557 - 1.903

*This performance indicator specifically refers to the temperature difference between the focal plane and the heat dissipation surface of the package structure.

Characteristics of the Temperature Sensor

This product uses a thermistor as the temperature sensor. Within the operating temperature range, the corresponding relationship between the thermistor's resistance value and temperature is shown in the figure below:



Typical Corresponding Relationship Between Thermistor Resistance and Temperature

Temperature (℃)	Resistance (kΩ)	Temperature (℃)	Resistance (kΩ)	Temperature (℃)	Resistance (kΩ)	Temperature (℃)	Resistance (kΩ)	Temperature (℃)	Resistance (kΩ)
-70	129.7	-45	29.40	-20	8.608	5	3.075	30	1.268
-65	94.27	-40	22.56	-15	6.909	10	2.550	35	1.077
-60	69.29	-35	17.49	-10	5.587	15	2.126	40	0.918
-55	51.50	-30	13.69	-5	4.549	20	1.782	45	0.786
-50	38.70	-25	10.81	0	3.729	25	1.500	50	0.674

Corresponding Relationship Between Thermistor Resistance and Temperature (Expressed by the Following Formula):

$$\frac{1}{(T_1+273.15)}=\frac{\ln\left(\frac{R_1}{R_2}\right)}{B}+\frac{1}{(T_2+273.15)}$$

T1: Test target temperature, Unit: ℃

T2: Reference point temperature, Unit: ℃. Within the range of -70~30℃, the typical values of reference temperature are -40℃ or -10℃, and a reference temperature value close to the target temperature should be selected.

R1, R2: Thermistor resistance values corresponding to T1 and T2 respectively, Unit: kΩ

B: Thermistor coefficient. Within the range of -70~30℃, the typical value of B-40/-10 is 2854.43 (with a deviation of ±2%), and the temperature deviation calculated from this typical value is ±0.5℃.

Notes

a) During the installation of the TEC, attention should be paid to the additional resistance introduced by the external electrical structure. If the additional resistance exceeds 10% of the TEC resistance, the I-V curve must be recalibrated.

b) It is recommended to connect the TEC in a way that minimizes the connection resistance. If pin soldering is necessary, short-circuit grounding protection should be implemented. The local temperature during pin soldering must be ≤ 250℃, and the soldering duration must be < 10s.

c) If higher measurement accuracy is required within a small temperature range, the B-value can be calculated independently as needed.

d) Before turning on the TEC, it is mandatory to confirm the following: the temperature sensor is working normally, the heat dissipation surface is in full contact with the heat sink, the heat dissipation surface meets the required

size, and the heat sink is functioning properly. It is not recommended to turn on the TEC without installing the heat sink or when the heat sink is not working.

e) When turning on the TEC for the first time, the current or voltage should be gradually applied starting from 0A or 0V. Meanwhile, monitor the temperature change until the preset temperature is reached.

f) Since the detector performance is affected by temperature, the TEC should be turned on first and stabilized at the target temperature before activating the detector. It is not recommended to operate the detector in an environment with fluctuating temperatures.

g) When the detector is not in use for an extended period, power supply to the TEC should be stopped to extend the TEC's service life.

h) The cooling effect of the detector is related to the ambient temperature, power supply performance, and heat dissipation status. It is recommended to properly match the heat dissipation system according to the actual operating environment and the required detector performance.

Product Support

Issue	Possible Causes	Solutions
Abnormal Signal Output of Detector	No power supply or abnormal power supply	Check if each power supply meets the electrical requirements specified in the manual.
	Abnormal timing	Adjust the detector's timing pulse width according to the recommended values in the manual.
	Short integration time or no light intensity	Increase the integration time and switch the gain level.
	Light intensity saturation	Shorten the integration time and switch the gain level.
Excessive Output Noise of Detector	High ripple noise of power supply	Supply power in accordance with the electrical requirements for DC power supply ripple noise in the manual.
	Reverse connection of TEC pins	Determine whether reverse connection exists by detecting with a temperature sensor.
	Noise introduction from backend electronic circuits	Inspect the layout of the board-level circuit structure and the status of circuit noise.